# InterPACK 2024

## International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems

# Program

**CONFERENCE**
**October 8-10, 2024**

**Holiday Inn San Jose, Silicon Valley**
**San Jose, CA**

https://event.asme.org/InterPACK

*The American Society of Mechanical Engineers®*
*ASME®*

ASME
SETTING THE STANDARD

# Dear InterPACK Participants,

On behalf of the ASME Electronic and Photonic Packaging Division (EPPD), we welcome you to the 2024 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems (InterPACK) being held at the Holiday Inn San Jose – Silicon Valley, San Jose, California, on October 8–10, 2024. This is an important and exciting time for Advanced Packaging as there is an increased focus on electronics manufacturing, specifically packaging for continued performance improvements and miniaturization.

The InterPACK Conference is a premier event organized by the ASME EPPD and holds a rich history of serving as a platform for exchanging information on cutting-edge research in the areas of electronic and photonic packaging, reliability, manufacturing, and thermal management of electronic devices, components, and systems by bringing together numerous researchers and technical professionals from Academia, Government, and Industry. The organizers have developed a comprehensive technical program comprised of more than 200 technical presentations and posters, including more than 90 original technical papers as well as tutorials, panel discussions, workshops, and plenary talks aligned with the areas of (i) heterogeneous integration; (ii) data centers and modular edge systems; (iii) electronics packaging; (iv) power/RF electronics and photonics; (v) multiscale thermal transport and energy storage; (vi) flexible, wearable, and printed electronics; and (vii) transportation systems, AI, and machine learning. The program has been organized to promote networking between government, academia, and industry researchers and professionals and to offer opportunities for fostering collaborations. Students will have an opportunity to present their work during the interactive presentation session and discuss their future career paths with senior researchers and industry leaders during a career panel.

We are pleased to announce that there will be a number of plenary talks from distinguished professionals in the area of electronic and photonic packaging, including Matthew Walsh (Naval Surface Warfare Center), John Oakley (Semiconductor Research Corporation), Art Wall (NextFlex National Manufacturing Institute), Radha Nagarajan (Marvell), Peter De Bock (ARPA-E, U.S. Department of Energy), Ani Natekar (Meta). In addition, the conference will have a number of keynotes, including John Thome (JJ Cooling Innovation), Adam Wilson (U.S. Army Research Laboratory), and Sheng Xu (UC San Diego). We will continue to promote research and development in the emerging areas of electronics and photonics that align with the goal of the ASME EPPD through the conference. We are pleased to host panel sessions and tutorials to discuss the trending topics in electronic and photonic packaging, thermal management, and reliability of electronic devices and electrified systems. In addition, we will host workshops dedicated to the recently announced CHIPS and Science Act and learn how the U.S. domestic semiconductor manufacturing, design, and research can be strengthened in the near future.

We hope that you will enjoy the program that has been organized by numerous volunteers contributing as track chairs, session chairs, workshop organizers, tutorial instructors, panel moderators, and technical paper reviewers. We are indebted to our volunteers as well as the ASME Staff for their vigorous and passionate efforts to make this conference a premier event. We also thank all our sponsors across the globe for their generous support as well as participation in the technical sessions.

**Prof. Pradeep Lall**
General Chair
*Auburn University*

**Dr. Saket Karajgikar**
Conference Chair
*nVidia*

**Dr. Jimil Shah**
Technical Program
*Stealth Mode Startup*

**Prof. Damena Agonafer**
Technical Program Co-Chair
University of Maryland

**Dr. Anna Prakash**
Sponsorship Chair
*Education Empowers*

**Dr. Ron Warzoha**
Award & Communication Chair
*United States Naval Academy*

## REGISTRATION HOURS AND LOCATION

**The hours are as follows:**

**MONDAY, OCTOBER 7**
3:00 PM – 6:00 PM

**TUESDAY, OCTOBER 8**
7:00 AM – 5:00 PM

**WEDNESDAY, OCTOBER 9**
7:00 AM – 5:00 PM

**THURSDAY, OCTOBER 10**
7:00 AM – 3:00 PM

**Location:** California Ballroom Foyer, Mezzanine Level

## AUDIO EQUIPMENT IN SESSION ROOMS

Each session room is equipped with a screen, LCD projector, and laptop. Speakers should arrive to their session room 10 minutes prior to the session start time. Bring a copy of your presentation on a USB/thumb-drive to be loaded onto the show computer.

## AUDIOVISUAL EQUIPMENT IN SESSION ROOMS

All technical sessions rooms are equipped with an LCD projector and screen. Laptops will NOT be provided in the sessions. Session chairs typically provide their laptops for all the author's presentations, or you may bring your own. Please bring your presentations on a jump drive 10–15 minutes before your presentation to upload it on the laptop provided by the session chair.

## BADGE REQUIRED FOR ADMISSION

All conference attendees must always wear the official ASME 2024 InterPACK badge to gain admission to technical sessions, exhibits, poster sessions, meals, and other conference events. Without a badge, you will NOT be allowed to attend any conference activities. Your badge also provides a helpful introduction to other attendees.

## CONFERENCE BREAKFAST

Complimentary Breakfast is offered Monday–Friday at the Santa Cruz Restaurant from 6:30AM to 9:30AM and on the weekends from 7:00AM to 10:00AM for all InterPACK attendees staying at the hotel. Available to one person per room.

## AIRPORT SHUTTLE

Complimentary shuttle to and from the San Jose International Airport is available. For pick up, please call the hotel and ask for pick-up, allow 5 to 10 minutes maximum to reach the airport. Pick-up times are from 5:00AM to 11:30PM.

## CONFERENCE AWARDS LUNCHEONS

2024 AVRAM BAR COHEN AWARD
Tuesday, October 8
12:15PM–1:30PM
California Ballroom – Salon FGHJ

ALAN KRAUS AWARD
Wednesday, October 9
12:15PM–1:30PM
California Ballroom – Salon FGHJ

InterPACK EPPD, JEP, AND NASSER GRAYELI POSTER AWARDS
Thursday, October 10
12:15PM–1:30PM
California Ballroom – Salon FGHJ

## CONFERENCE NETWORKING BREAKS

Morning and afternoon breaks will be provided in the Royal Foyer located on the First Floor. Join your fellow attendees for a few minutes of networking and discussion. The schedule is as follows:

Tuesday, October 22 to Thursday, October 24
10:45AM–11:00AM and 2:15PM–2:30PM

## CONFERENCE PROCEEDINGS

Each attendee will be provided with an individual link to the online papers via email. In the event you do not receive the email, send a request to conferencepubs@asme.org. Access to all the papers accepted for presentation at the conference will be found online with this link. The official conference archival proceedings will be published after the conference and will not include accepted papers that were not presented at the conference. The official conference proceedings are registered with the Library of Congress and are submitted for abstracting and indexing .The proceedings are published in the ASME Digital Library and are available for a fee.

## REGISTRANTS WITH DISABILITIES

Whenever possible, we are pleased to plan for registrants with disabilities. Advance notice may be required for certain requests. For on-site assistance, please visit the conference registration area and ask to speak with a conference representative.

## CONFERENCE APP

The InterPACK 2024 Symposium will be utilizing the ASME Conferences mobile app to enhance the experience for attendees and speakers in place of a printed program. Connect with Attendees, View Speaker Profiles, Access Session Information, and more!

## INTERNET ACCESS

Basic complimentary sleeping room Wi-Fi will be provided for you if you are staying at the Holiday Inn San Jose – Silicon Valley. You will be given a Wi-Fi code to use in your sleeping room during your stay.

ASME has provided Wi-Fi access in the meeting space, here is the network information and code:

Network Name: IHG One Rewards
Access Code: SJCCC

## MEMBERSHIP TO ASME (4 MONTHS FREE)

Registrants who paid the non-member conference registration fees will receive a four-month complimentary ASME Membership. ASME will automatically activate this complimentary membership for qualified attendees. Please allow approximately four weeks after the conclusion of the conference for your membership to become active.

Visit www.asme.org/membership for more information about the benefits of ASME Membership.

## PRESENTER ATTENDANCE POLICY

According to ASME's Presenter Attendance Policy, if a paper is not presented at the conference, the paper will not be published in the official Archival Proceedings, which are registered with the Library of Congress and are abstracted and indexed. The paper also will not be published in the ASME Digital Collection and may not be cited as a published paper.

## ABOUT THE HOTEL

Stylish hotel accessible to Downtown San Jose
The Holiday Inn San Jose – Silicon Valley, an IHG hotel is located 2 miles from San Jose International Airport SJC. Minutes from downtown San Jose, this pet friendly contemporary hotel reflects the unique energy of California's thriving Bay Area. Step inside their warm and welcoming ambiance making you feel right at home.

Unwind in their inviting accommodations that feature modern amenities. Drink and dine in style at our newly renovated on-site restaurant and Pub featuring breakfast and dinner specialties. The Pub is open Monday–Sunday, 5:00PM–10:00PM. Featured amenities include a 24-hour business center, dry cleaning/laundry services, complementary parking, and a 24-hour front desk. A 24-Hour Market Pantry is available for grab and go snacks.

Their convenient location gives easy access to I-880, I-280, and Highway 101. Take advantage of the light rail system adjacent to the hotel. Visit popular points of interest including Kaiser Permanente San Jose Medical Center, Kaiser Permanente Hospital, Regional Medical Center and Operation Warp Speed distribution locations.

Each guestroom features flat-screen televisions, complimentary wireless internet access keeps you connected, and cable programming is available for your entertainment. Bathrooms have shower/tub combinations and hair dryers. Conveniences include phones, as well as desks and irons/ironing boards.

Enjoy recreational amenities such as an outdoor pool and a 24-hour fitness center. Additional features at this hotel include complimentary wireless internet access, and gift shops/newsstands. Enjoy a satisfying meal at Santa Cruz Restaurant serving guests of Holiday Inn San Jose – Silicon Valley, an IHG Hotel. Wrap up your day with a drink at the bar/lounge.

At the Holiday Inn San Jose – Silicon Valley, an IHG Hotel, you'll be within a 5-minute drive of PayPal Park and SAP Center at San Jose. This hotel is 2.5 mi (4 km) from The Tech Interactive and 2.7 mi (4.3 km) from San Jose Convention Center.

## EMERGENCY INFORMATION

- In case of a medical emergency, Dial 911 from any house phone.
- In case of a non-life-threatening emergency, Dial 0 from any house phone.
- In the unlikely event of an emergency, there will be an announcement over the public address of what the particular incident is and providing further instruction as far as whether to evacuate or remain in place. All employees are familiar with evacuation procedures and will assist in giving directions.
- In the unlikely event of a fire emergency, visual strobes will activate with audible alarms, followed by an announcement over the public address of what the particular incident is and providing further instruction as far as whether to evacuate or remain in place. All employees are familiar with evacuation procedures and will assist in giving directions.
- Do not take elevators and follow all instructions given.

## ABOUT SAN JOSE, CALIFORNIA AND SILICON VALLEY

San Jose, also known as the "Capital of Silicon Valley," is a vibrant city nestled in the heart of California. With a population of over one million residents, San Jose is the third-largest city in the state and the tenth largest in the entire United States.

Known for its bustling technology industry and innovative spirit, San Jose is home to numerous tech giants and startups that have revolutionized the world. But there's more to this city than just technology. From its rich history to its diverse culture, San Jose has something to offer everyone.

Some Interesting Facts About San Jose

- The Muwekma Ohlone — the Tamyen people — were the original inhabitants of what is now San Jose.
- San Jose's full name was El Pueblo de San Jose de Guadalupe.
- It was a farming community.
- It was once the capital of California.
- It was the site of California's Largest Mercury Mine.
- It was a supply station during the Gold Rush.
- The city once housed the world's largest canning and dried-fruit packing center.
- San Jose is the largest city in Northern California.
- Many celebrities hail from San Jose, such as Steve Wozniack, Dustin Diamond, Scott Weiland, and Kate Walsh.
- San Jose is the home of innovation.

# Schedule at a Glance

| From | To | Room/Event | Type |
|---|---|---|---|
| **Time** | | **Day 1: Monday — October 7, 2024** | |
| 3:00PM | 6:00PM | Location: California Ballroom Foyerr, Mezzanine Level | ASME Meetings |
| | | Registration Opens | ASME Meetings |
| 6:30PM | 8:30PM | Location: TBD | ASME Meetings |
| | | Leadership Dinner - By invitation Only | ASME Meetings |

| From | To | Room/Event | | | | Type |
|---|---|---|---|---|---|---|
| **Time** | | **Day 2: Tuesday — October 8, 2024** | | | | |
| 7:45AM | 8:00AM | Room: California DE | | | | ASME Meetings |
| | | InterPACK'24 -Opening Remarks by Prof. Pradeep Lall | | | | ASME Meetings |
| 8:00AM | 8:45AM | Room: California Ballroom , Salons FGHJ | | | | Plenary Speaker |
| | | OUSD IBAS RESHAPE Project - Matthew Walsh | | | | Plenary Speaker |
| 8:45AM | 9:30AM | The Use of Additive Hybrid Electronics as a Key Element in the National Strategy for Advanced Packaging - Art Wall | | | | Plenary Speaker |
| 9:30AM | 10:45AM | Room: Califnornia Ballroom, Salon C | Room: California Ballroom, Salon B | Room: California Ballroom, Salon K | Room: California Ballroom, Salon A | Technical Sessions |
| | | 03-01: Electronics Packaging - Electrical Design | 02-01: Data Centers and Modular Edge Systems - I | 07-01: Transportation Systems, AI and Machine Learning - I | Reliability of Additively Manufacturing Flexible and Stretchable Electronics – Experiments, Models, and Applications | Workshops |
| 10:45AM | 11:00AM | Coffee Break/Exhibitors - California Ballroom, Mezzanine Foyer | | | | |
| 11:00AM | 12:15PM | Room: California Ballroom, Salon C | Room: California Ballroom, Salon L | Room: California Ballroom, Salon M | Room: California Ballroom, Salon A | Technical Sessions |
| | | 03-02: Electronics Packaging - Components | 04-01: Power/RF Electronics and Photonics - I | 06-01: FHE Design & Reliability | Data Center and Telecom Challenges and Opportunities | Panel |
| 12:15PM | 1:30PM | Room: California Ballroom, Salons FGHJ | | | | Lunch Presentations |
| | | Lunch: Avram Bar-Cohen Award | | | | Lunch Presentations |
| 1:30PM | 2:15PM | Room: California Ballroom, Salon D | | Room: California Ballroom, Salon E | | Track Keynotes |
| | | Passive Two-Phase Cooling of Electronics and Energy Efficiency | | Efficient Energy Systems | | Tutorials |
| 2:15PM | 2:30PM | Coffee Break/Exhibitors - California Ballroom, Mezzanine Foyer | | | | |
| 2:30PM | 3:45PM | Room: California Ballroom, Salon C | Room: California Ballroom, Salon B | Room: California Ballroom, Salon L | Room: California Ballroom, Salon A | Technical Sessions |
| | | 03-04: Electronics Packaging - Stress and Reliability - I | 02-02: Data Centers and Modular Edge Systems - II | 04-02: Power/RF Electronics and Photonics - II | Machine Learning for Electronics | Panel |
| 3:50PM | 5:15PM | Room: California Ballroom, Salon C | Room: California Ballroom, Salon M | Room: California Ballroom, Salon K | Room: California Ballroom, Salon A | Technical Sessions |
| | | 03-05: Electronics Packaging - Stress and Reliability- II | 06-02: Advanced Materials & Processes for Printed Electronics - I | K16 Mentorship | Women in Engineering | Workshops |
| | | Room: California Ballroom, Salon L | | | | Short Course |
| | | Short Course - Efficient Thermal Simulations Using Compact Models | | | | Short Course |
| 5:45PM | 6:45PM | Room: Salon San Jose Ballroom | | | | Student Posters |
| | | Interactive Poster Session | | | | Student Posters |
| 6:45PM | 7:15PM | Room California Ballroom, Salon D | | | | ASME Meetings |
| | | JEP Editorial Meeting | | | | ASME Meetings |
| 7:15PM | 8:45PM | Room: California Ballroom, Salon D | | | | ASME Meetings |
| | | K-16 Committee Meeting (Open) | | | | ASME Meetings |
| 8:45PM | 9:15PM | Room: California Ballroom, Salon D | | | | ASME Meetings |
| | | K-16 Committee Meeting (Closed) | | | | ASME Meetings |

| From | To | Room/Event | Type |
|---|---|---|---|
| **Time** | | **Day 3: Wednesday — October 9, 2024** | |
| 8:00AM | 9:30AM | Room: California Ballroom , Salons FGHJ | Plenary Speaker |
| | | 2.5D/3D Integration for High-Speed Light Engines - Radha Nagarajan | Plenary Speaker |

| | | | | | | |
|---|---|---|---|---|---|---|
| | 10:45AM | Room: California Ballroom, Salon C | Room: California Ballroom, Salon A | Room: California Ballroom, Salon M | Room: Salon K | Technical Sessions |
| | | 03-06: Electronics Packaging - Stress and Reliability - III | 01-01: Heterogeneous Integration | 06-04: Materials & Processes for RF Electronics | Liquid-Cooling and Heat Reuse Technologies | Tutorials |
| 10:45AM | 11:00AM | Coffee Break/Exhibitors - California Ballroom, Mezzanine Foyer | | | | |
| 11:00AM | 12:15PM | Room: California Ballroom, Salon C | Room: California Ballroom, Salon B | Room: California Ballroom, Salon M | Room : California Ballroom, Salon K | Technical Sessions |
| | | 03-07: Electronics Packaging - Stress and Reliability - IV | 02-03: Data Centers and Modular Edge Systems - III | 06-05: FHE Applications & Processing | Advancing Electronics Packaging and Heterogeneous Integration: Insights | Workshop |
| 12:15PM | 1:30PM | Room: California Ballroom, Salons FGHJ | | | | Lunch Presentations |
| | | Lunch: InterPACK'24 Allan Kraus Award | | | | |
| 1:30PM | 2:15PM | Room: California Ballroom, Salon D | | Room: California Ballroom, Salon E | | Track Keynotes |
| | | Size and Timescale Matching for Transient-Aware Thermal Management | | AI/ML and Industry Trends | | Tutorials |
| 2:15PM | 2:30PM | Coffee Break/Exhibitors - California Ballroom, Mezzanine Foyer | | | | |
| 2:30PM | 3:45PM | Room: California Ballroom, Salon C | Room: California Ballroom, Salon B | Room: California Ballroom, Salon K | Room : California Ballroom, Salon A | Technical Sessions |
| | | 03-08: Electronics Packaging - Reliability | 02-04: Data Centers and Modular Edge Systems - IV | [redacted] | Thermal/Mechanical/Electrical Challenges and Opportunities for | Panel |
| 3:50PM | 5:15PM | Room: California Ballroom, Salon L | Room: California Ballroom, Salon M | Room: California Ballroom, Salon C | | Technical Sessions |
| | | 05-03: Multiscale Thermal Transport and Energy Storage - III | 06-06: Advanced Materials & Processes for Printed Electronics - II | 03-09: Electronics Packaging - Thermal - I | | Workshops |
| 6:00PM | 6:30PM | Room: California Ballroom, Salon D | | | | ASME Meetings |
| | | InterPACK Meeting (Closed) | | | | |
| 6:30PM | 7:00PM | Room: California Ballroom, Salon D | | | | ASME Meetings |
| | | InterPACK Meeting (Open) | | | | |
| 7:00PM | 8:00PM | Room: California Ballroom, Salon D | | | | ASME Meetings |
| | | EPPD Meeting (Open) | | | | |

| Time | | Day 4: Thursday — October 10, 2024 | | | | |
|---|---|---|---|---|---|---|
| From | To | Room/Event | | | | Type |
| 8:00AM | 8:45AM | Room: California Ballroom , Salons FGHJ | | | | Plenary Speaker |
| | | ARPA-E COOLERCHIPS Technology for a Future of Energy Efficient High Power Density/AI Data Centers - Peter de Bock | | | | |
| 8:45AM | 9:30AM | Data Center Industry's Supply Chain Readiness and Scalability for Liquid Cooling - Ani Natekar | | | | |
| 9:30AM | 10:45AM | Room: California Ballroom, Salon C | Room: California Ballroom, Salon L | Room: California Ballroom, | Room: California Ballroom, Salon M | Technical Sessions |
| | | 03-10: Electronics Packaging - Thermal - II (Two-phase) | 05-01: Multiscale Thermal Transport and Energy Storage - I | 02-05: Data Centers and Modular Edge Systems - V | Status, Challenges, and Opportunities in Electronics Packaging from a | Workshop |
| 10:45AM | 11:00AM | Coffee Break/Exhibitors - California Ballroom, Mezzanine Foyer | | | | |
| 11:00AM | 12:15PM | Room: California Ballroom, Salon C | Room: California Ballroom, Salon L | Room: California Ballroom, | Room: California Ballroom, Salon M | Technical Sessions |
| | | 03-11: Electronics Packaging - Thermal - III | 05-02: Multiscale Thermal Transport and Energy Storage - II | 02-07: Data Centers and Modular Edge Systems - VII | Additive Manufacturing for Domestic Electronics Packaging | Panel |
| 12:15PM | 1:30PM | Room: California Ballroom, Salons FGHJ | | | | Lunch Presentations |
| | | "Lunch: ASME Worcester Reed Warner Medal + InterPACK'24 Awards (Nasser Grayeli Poster, EPPD, JEP)" | | | | |
| 1:30PM | 2:15PM | Room: California Ballroom, Salon D | | Room: California Ballroom, Salon E | | Track Keynotes |
| | | Wearable Ultrasound Technology | | Additive Manufacturing for Electronic Devices and Interconnects | | Tutorials |
| 2:15PM | 2:30PM | Coffee Break/Exhibitors - California Ballroom, Mezzanine Foyer | | | | |
| 2:30PM | 3:45PM | Room: California Ballroom, Salon C | Room: California Ballroom, Salon B | Room: California Ballroom, Salon M | Room: California Ballroom, Salon A | Technical Sessions |
| | | 03-12: Electronics Packaging - Thermal IV (Single Phase Convection) | 02-06: Data Centers and Modular Edge Systems -VI | 06-07: FHE Printing & Packaging | Two-phase Flow for Electronics Cooling | Panel |
| 3:50PM | 5:15PM | | | | Room: California Ballroom, Salon M | Technical Sessions |
| | | | | | 06-03: Printed Electronics for Wearables & Health | Workshop |

# SPONSORS AND EXHIBITORS

## PLATINUM SPONSOR

**National Renewable Energy Laboratory (NREL)** researchers within the Advanced Power Electronics & Electric Machines (APEEM) Group have expertise in thermal, electrothermal, mechanical, and reliability of power electronics and electric machines for energy efficiency and renewable energy applications, such as electric-drive vehicles. In collaboration with research and industry partners, NREL's APEEM Group is developing novel thermal management technologies to improve the performance, cost, reliability, and volume of power electronics and electric machines. NREL has five facilities dedicated to APEEM research, featuring a range of equipment to investigate primary research areas of 1) electronic and power electronic devices and sensors, 2) power electronics thermal management, 3) power electronics packaging reliability and prognostics, 4) electric motor thermal management, 5) integrated electric drive thermal management.

**Learn more about the capabilities and facilities at NREL on our website.**

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## GOLD SPONSORS

**The University of Texas at Arlington** is a Carnegie Research Institution (High Research Activity) whose mission is the advancement of knowledge and the pursuit of excellence in research, teaching, and service to the community. The mission statement affirms UT Arlington's commitment to expanding academic research; to attracting and retaining high quality faculty scholars who actively engage students; to providing a well-rounded academic experience that promotes student involvement, service learning, and free discourse; to employing alternative access venues to meet student's needs; and to developing public and private partnerships.

**College of Engineering**

The University of Texas at Arlington's College of Engineering has emerged as one of the most comprehensive engineering programs in North Texas and the nation. It offers 11 baccalaureate, 14 master's, and nine doctoral degree programs, and its programs are ranked by U.S. News and World Report as among the best in the nation. With more than 7,500 students and more than 34,000 alumni, the College of Engineering is the fourth largest in Texas, providing the local, regional, and national workforce with motivated and highly skilled graduates. The College boasts seven buildings, including the Science and Engineering Innovation and Research (SEIR) Building, which opened in Fall 2018. UTA is classified as a Research 1 University.

Electronics, MEMS and Nanoelectronics Systems Packaging Center National Academy of Engineering, the Electronics, MEMS and Nanotechnology Systems Packaging Center is a first-class research center that will meet the needs of industry, and in particular, the state of Texas and the North Texas region's Electronic, MEMS and Nanoelectronics Packaging Industry.

This includes research, education, and training. EMNSPC will target the needs of the Microelectronics, MEMS and Nanoelectronics (with a special emphasis on thermo-mechanical issues) as a fundamental research area as these technologies have and will continue to overlap. The EMNSPC is a partner in the NSF I/UCRC Center for Energy-Smart Electronic Systems, working with government, industry, and academia to develop systematic methodologies for efficiently operating electronic systems. More information at**: https://blog.uta.edu/emnspc/**

Staubli is a leading global manufacturer of quick-release coupling systems for use in IT/liquid cooling. Our products have been designed for perfect integration in installations such as data centers or super computers. Staubli North America has more than 200 employees supporting

Connectors, Robotics, and Textiles customers. The company's North American headquarters is in Duncan, South Carolina. Staubli has a global workforce of over 6,000 employees, 15 production sites across the globe, and is supported by a comprehensive distribution network in 50 countries worldwide. URL: https://www.staubli.com/us/en/fluid-connectors/industries/it-telecom-broadcasting.html

## SILVER SPONSORS

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When visionary companies need to know how their world-changing ideas will perform, they close the gap between design and reality with Ansys simulation. For more than 50 years, Ansys software has enabled innovators across industries to push boundaries by using the predictive power of simulation. From sustainable transportation to advanced semiconductors, from satellite systems to life-saving medical devices, the next great leaps in human advancement will be powered by Ansys. Learn more at ansys.com.

**Website Link:** http://www.ansys.com/

**General Sponsor**

Georgia Institute of Technology (Georgia Tech) has strong academic and research programs in multi-scale thermal management of microsystems. These span from semiconductor device level to large scale data centers. Ongoing efforts focus on fundamental investigations, as well as emerging technologies related to three-dimensional heterogeneous integration, high performance computing, power electronics, electric machines, and energy storage for transport electrification, and evaporative cooling for data centers. Examples of ongoing research from the METTL and MiNDS labs are included below.

**To find out more about Stanford University, please visit:**

https://nanoheat.stanford.edu/

**Microsanj** is a leading supplier of high resolution, thermal Imaging systems, tools, and consulting services. Microsanj imaging systems support thermoreflectance-based and infrared-based imaging coupled with digital signal processing and advanced patented software algorithms to support microelectronic component thermal characterization for thermal design validation, defect analysis, and reliability analysis. Microsanj currently offers the highest resolution thermal imaging systems on the market. For more information visit: For more information visit: **www.microsanj.com**

**Novark Technologies, Inc**. leverages nearly two decades of experience and expertise in thermal management solutions of electronics. Its product lines include various heat pipe, vapor chamber, heat column, heat sink, liquid cooling, two-phase cooling and other advanced thermal solutions used in a variety of electronics cooling applications ranging from CPU and GPU to data center to industrial power systems to telecommunications to EV thermal management solutions and more. Routine support of academic research at various institutions in the US, Europe and China combines with constant exploration of new thermal management solutions to push the company's capabilities forward continuously.

Founded in 2008, the **Toyota Research Institute of North America (TRINA)** is exploring next-generation core technologies via fundamental research discoveries that enable breakthrough applications for a sustainable mobility society. TRINA is building the foundation for Toyota's advanced product development through in-house research plus collaborative efforts with both internal and external partners across North America which has resulted in more than 1,200 granted patents and numerous high impact publications since inception.

Link: Toyota Research Institute of North America (TRINA) - AMRD

# SPONSORS AND EXHIBITORS

## SILVER SPONSORS

**The Journal of Electronic Packaging** publishes papers that use experimental and theoretical (analytical and computer-aided) methods, approaches, and techniques to address and solve various mechanical, materials, and reliability problems encountered in the analysis, design, manufacturing, testing, and operation of electronic and photonics components, devices, and systems.

The journal publishes papers that address: 1) thermal management, applied mechanics and technologies for microsystems packaging; 2) critical issues in systems integration; 3) emerging packaging technologies and materials with micro/nano structures; and 4) general small-scale systems.

The journal serves researchers and engineers working in academic and industrial settings. In addition, leaders in the field are invited to publish review articles on hot, emerging, and fundamental topics.

**Scope:** Electronic packaging; Thermal management; Applied mechanics; Microsystems packaging; Systems integration; Small scale systems in general.
https://asmedigitalcollection.asme.org/electronicpackaging.

**Contact:**

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**Purdue University.**

**Semiconductor Packaging Laboratory**

*(All-in-one for Semiconductor Packaging, Heat transfer, and Assembly Lab)*

**The Semiconductor Packaging Laboratory (SPACK)** at Purdue University, led by Professor Tiwei Wei, focuses on addressing fabrication challenges in semiconductor packaging and assembly, as well as related heat transfer issues. The lab's research can be broadly categorized into two main areas:

1. Materials, Processing, and Architecture Development for Semiconductor Packaging: This involves investigating new thermal, mechanical stress, and electrical behaviors in scaling 3D interconnects or developing novel materials for vertical 3D interconnects.
2. Chip/Package Level Thermal Management: This includes electronic cooling techniques at both chip and package levels, such as jet cooling and microchannel cooling. It also encompasses surface engineering to enhance advanced cooling technologies, as well as thermal modeling, analysis, and management of advanced packaging solutions.

**For more information visit our lab link:** https://s-pack.org/

**Contact:**

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Purdue University
Email: tiwei@purdue.edu

## SILVER SPONSORS

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**Element Six (E6)** designs, develops, and produces world-leading synthetic diamond and tungsten carbide solutions at a global scale.

Since 1946, E6's focus has been on engineering and optimizing the diamond synthesis process to unlock innovative, diamond-enabled applications, including ultra-precision machining, drilling, thermal management, optics and photonics, wastewater management and quantum-enabled sensing.

Element Six pioneered the development of single crystal diamond using the Chemical Vapor Deposition (CVD) method in the early 2000s.

With CVD production facilities in the US and UK, the company has been at the forefront of a range of new developments in CVD diamond synthesis and associated industrial applications.
E6's patented technologies also drive what is believed to be the world's largest CVD manufacturing site, based in Oregon, US.

Working closely with a network of global collaborators, E6's diamond solutions have accelerated the delivery of many breakthroughs in quantum research, including:

- In 2012, Harvard reported isotopically engineered CVD single crystal achieved spin coherence times of seconds at room temperature.
- Alongside TU Delft in 2015, E6's materials enabled the first successful loophole-free Bell's inequality test, proving for the first time that 'spooky action at a distance' is real. This also marked a significant technology step toward a quantum-secure enabled network.
- In 2018, Imperial College London utilized E6's engineered single crystal in the development of the world's first continuous-wave, room-temperature, solid-state MASER.
- Lockheed Martin's 2019 'Dark Ice' program delivered a DNV-enabled magnetometer that measured the direction and strength of nearly imperceptible magnetic field anomalies, opening up diamond-based quantum devices in GPS-denied navigation.

**Our website:** Element Six | Synthetic Diamond and Tungsten Carbide Experts - Element Six (e6.com)

NEIT
NANOSCALE ENERGY AND INTERFACIAL TRANSPORT

UNIVERSITY OF MARYLAND 1856
A. JAMES CLARK
SCHOOL OF ENGINEERING

**NEIT Lab:** https://neit.umd.edu/
**UMD ME engineering:** https://enme.umd.edu/

The **NEIT Lab's** research group is dedicated to advancing the field of thermal-fluid sciences, interfacial transport phenomena, and renewable energy. The group's efforts are centered on developing innovative materials and systems for the thermal management of power and microelectronic systems and for thermochemical and electrochemical energy storage. By tuning and controlling solid-liquid-vapor interactions at micro- and nanoscale levels, the group aims to achieve transformational technological advancements. Their research spans a wide range of applications, including cooling high-powered electronics, managing battery thermal conditions, improving data center cooling, and enhancing the efficiency of HVAC systems.

**NEIT Lab** URL: https://neit.umd.edu/
**UMD**: https://enme.umd.edu/
**CALCE:** https://calce.umd.edu/

**Georgia Institute of Technology**
Logo and Summary to follow

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S3IP brings together teams of experts from industry and academia to address pressing real-world problems in electronics manufacturing. Our research centers focus on packaging and thermal management, heterogeneous integration, energy-efficient electronic systems and energy harvesting and storage. Li-ion battery research is conducted by Dr. M. Stanley Whittingham, 2019 Nobel Laureate. Binghamton University, the premier public university in the Northeast, is home to S3IP, a New York State Center of Excellence. Our PhD-degreed staff members and affiliated faculty, in 6 constituent research centers and 9 laboratories, are ready to assist companies with collaborative problem solving. As a result of our combined efforts, our industry partners have reported over $1.9 billion of economic benefit. Binghamton.edu/s3ip

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Short Course
Tuesday, October 8
3:30PM–5:15PM
California Ballroom, Salon L, Mezzanine Level

Presentation: Efficient Thermal Simulations Using Compact Models

**SUMMARY**

Heat is generated in almost all technical processes. For example, the integration density in modern electronic systems is so high that their performance is limited by cooling. Microelectronic reliability depends on thermo-mechanical properties of packages. Highly integrated batteries of hybrid electrical vehicles depend on cooling. The properties of electrical machines are determined by the heat losses, etc. These effects can be determined by numerical simulations via e.g., finite element analysis of temperature fields. However, the key to correctly considering the entire system is a system-level simulation in which compact thermal models are connected to further mechanical, electrical or fluidic components.

Furthermore, the compact models can be used for efficient design optimization and control and can be shared along the supply chain, as they protect the IP.

Using industry-relevant examples, this seminar shows the great advantages of compact thermal models, explains the underlying theory in a comprehensive way and presents the state-of-the-art software tools and working flow.

**INSTRUCTOR**

**Tamara Bechtold** obtained her PhD in microsystem simulation from the University of Freiburg, Germany, in 2005. Between 2006 and 2010, Dr. Bechtold worked as a research engineer for Philips Research Laboratories and NXP Semiconductors in Eindhoven, The Netherlands. The objective of her research work was to enhance the standard IC design flow through model order reduction and optimization modules. From 2011 to 2014 she acted as an interim Professor for microsystems simulation at the University of Freiburg, Germany and since 2014 as a lecturer and research group leader at the University of Rostock, Germany. Since 2017 Dr. Bechtold is a full professor for mechatronic systems at **Jade University** of applied sciences in Wilhelmshaven, Germany. Since 2022 she is a managing director of **Steinbeis Transfer Center Finite Element Simulation, Model Order Reduction and Design Optimization.**

Dr. Bechtold is author or co-author of over 150 technical publications in the area of modelling and simulation of micro-mechatronic systems, the lead author of the textbook “Fast Simulations of Electro-Thermal Microsystems: Efficient Dynamic Compact Models”, published by Springer and the main editor of the textbook “System-Level Modeling of MEMS”, by Wiley-VHC book series on Advanced Micro and Nanosystems. Her research interests cover applications of advanced mathematical methods of model order reduction and topology optimization to engineering problems and a multi-physics modelling on the device- and system-level.

**TUESDAY, OCTOBER 8**
8:00 AM–9:30 AM
CALIFORNIA BALLROOM DE, MEZZANINE LEVEL

**Matthew Walsh**
*Industrial Base Analysis and Sustainment (IBAS)*
*Naval Surface Warfare Center*
Crane, IN

**Matthew Walsh** is the Advanced Packaging Chief Engineer, Industrial Policy, Industrial Base Analysis and Sustainment (IBAS) Program Office of the Assistant Secretary of Defense for Industrial Base Policy. He is the technical lead on the Secure Advanced Packaging project within the Reshore Ecosystem for Secure Heterogeneous Advanced Packaged Electronics (RESHAPE) effort, and technical SME for other microelectronics projects within the OSD IBAS. Within the Navy, Matt was Advanced Radars Chief Engineer developing advanced packaging technologies for advanced radars, electronic warfare, and communication sensors. Matt has been in the electronics industry since 1988 with most of those years in the industry developing IC packaging technologies, powertrain electronics, radar sensors and harsh environment electronics for automotive and commercial vehicles. He has 13 published papers, 8 patents and 4 defensive publications in the automotive world, and 5 patents with the Navy.

**Presentation Title:** OUSD IBAS RESHAPE Project

**Abstract:** As microelectronic technology developments occurred in the 1980s and 1990s, it was perceived that packaging technologies became very mature and did not require new developments. Therefore, the majority of microelectronics packaging manufacturing was off shored to China and Pacific Rim countries such as Singapore, Malesia, Taiwan, Hong Kong, Indonesia for their low-cost labor and the absence of environmental restrictions to manufacturing. The microelectronics packaging industry since this off-shoring has remained being seen as mature with no requirements for developments and thus remains off-shore. With Moore's Law coming to an end for IC processing, and a continuing need to reduce SWaP-C and increase performance, the introduction of 2.5-D and 3-D Advanced Packaging has become a focal point for DoD and Commercial applications. It is now in the forefront of development activities worldwide. As the microelectronics evolution progresses, circuit feature sizes decrease to accommodate the need for high-density packaging. Theoretical feature size limits in the 2-D space and the cost to increase wafer size forces suppliers to move towards 3-D heterogeneous architectures. Integrating ICs from multiple technology nodes to increase cost-efficiency by only fabricating the components that need the highest performance, power advantage, and area savings in the latest node technology, while fabricating other system components at cheaper nodes. Improvements in advanced packaging is required for seamless integration. Although the European and Asian semiconductor industries have embraced these developments, no single country has emerged as a front-runner in the development and scale-up of advanced microelectronics 3-D packaging technologies and manufacturing processes. This provides an opportunity for the U.S. to advance as a worldwide leader, developer, and supplier of these foundational and dual-use technologies.

The focus of the OUSD IBAS RESHAPE (Re-shore Ecosystem for Secure Heterogeneous Advanced Packaged Electronics) effort is to develop a domestic, trusted, pure-play and open-access advanced packaging manufacturing ecosystem for low-volume/high-mix production of 2.5-D and 3-D Advanced System Integration and Packaging (ASIP) secure solutions. This prototype effort relates to foundational Advanced Packaging manufacturing capabilities required for advanced system integration of microelectronics packages including the following:

- Wafer Preparation
- Wafer Bumping
- Silicon Interposer Fabrication
- III/V Interposer Fabrication
- Classified Interposer Assembly
- Advanced Test and Failure Analysis Capability
- Fan-Out Wafer-Level Packaging
- Wafer-Level High-Density Interconnects
- Advanced Thermal Technologies
- Specialized Packaging for RF and Photonics
- Assembly Design Kits (ADKs) for SOTA Computer-Aided Design (CAD) Tools

**TUESDAY, OCTOBER 8**
8:00 AM–9:30 AM
CALIFORNIA BALLROOM DE, MEZZANINE LEVEL

**Art Wall**
*Director of Engineering & Fab Operations*
*NextFlex*
San Jose, CA

**Art Wall** is the Director of Engineering and Fab Operations at NextFlex, managing the Technology Hub which houses multiple novel electronics manufacturing capabilities for Flexible Hybrid Electronics development and prototyping, a novel new way of producing electronics devices. Prior to joining NextFlex, Art led many different groups of organizations and technologies associated with hard drive products for both IBM and Hitachi Global Storage Technologies. His most recent efforts prior to joining NextFlex were as a co-founder and Vice President of NuvoSun, an innovative thin film photovoltaic company that was acquired by The Dow Chemical Company. Art has a Ph.D. in Materials Science from the University of Minnesota, has co-authored more than 30 articles in refereed journals, presented at more than 20 U.S. and International Conferences, and holds 7 U.S. patents.

**Presentation Title:** The Use of Additive Hybrid Electronics as a Key Element in the National Strategy for Advanced Packaging

**Abstract:** There are many challenges and opportunities for the use of additive or printed electronic interconnect to packaging. The manufacturing opportunities include significantly lower cost of entry, inherently fewer process steps, wide variety of materials options, reduced impact on waste, water and power, and the opportunity for viable low volume, high mix electronic device production. The technology is still evolving with some notable innovations that can have a large impact on the future capability. In some cases, these can be disruptive but need further maturity. In the end, reliable solutions to integrated high resolution printing and economical multilayer processes are required to have the greatest impact on electronic advanced packaging.

**WEDNESDAY, OCTOBER 9**
8:00 AM–9:30 AM
CALIFORNIA BALLROOM DE, MEZZANINE LEVEL

**Radha Nagarajan**
SVP and CTO
Marvell's Optical and Cloud Connectivity Group
Santa Clara, CA

**Radha Nagarajan** is currently the Senior Vice President and Chief Technology Officer of Marvell's Optical and Cloud Connectivity Group. At Marvell, he manages the development of the company's optical platform technology and products. Concurrently, he is a Visiting Professor at the Department of Electrical and Computer Engineering at the National University of Singapore. He received his B.Eng. from the National University of Singapore, M.Eng. from the University of Tokyo, Japan, and Ph.D. from the University of California, Santa Barbara, USA, all in Electrical Engineering. Dr. Nagarajan's other recognitions include the IEEE/LEOS Aron Kressel Award, the IPRM Award and the Optica David Richardson Medal for breakthrough work in the development and manufacturing of photonic integrated circuits. He was named to Electro Optics' The Photonics100 in 2024, which honors the industry's most innovative people. He has been awarded more than 245 U.S. patents and is a Fellow of Optica, IEEE, and IET.

**Presentation Title:** 2.5D/3D Integration for High-Speed Light Engines

**Abstract:** Massive deployments of AI data centers have rapidly pushed the speed of optical interconnects from 800Gbit/s to 1.6Tbit/s and beyond, while placing a premium on power, performance, and latency. In this talk, we discuss the use of 3D heterogeneous integration, on silicon photonics, to enable low energy, high density high speed optical interconnects for these applications. Heterogeneous optical integration in this talk is where separately manufactured electronic components and semiconductor lasers are assembled on to an active silicon photonics interposer to form a Light Engine. This process allows for the integration of components independently designed and optimized from several different technology and foundry platforms onto a common interposer.

**THURSDAY, OCTOBER 10**
8:00 AM–9:30 AM
CALIFORNIA BALLROOM DE, MEZZANINE LEVEL

**Peter de Bock**
*Program Director*
*Advanced Research Projects Agency-Energy (ARPA-E)*
*U.S. Department of Energy*

**Peter de Bock** currently serves as Program Director at the Advanced Research Projects Agency-Energy (ARPA-E) for the US Department of Energy. At ARPA-E, Dr. de Bock developed the COOLERCHIPS program focused on making a transformational leap in efficiency of cooling of Data Center and leads and developed the ASCEND and PRE-TRAILS programs to realize a future of sustainable aviation. In addition, Dr. de Bock manages projects in the areas of ultra-high power density battery systems, hydrogen storage and propulsion, additive manufacturing and power electronics. Prior to joining ARPA-E, Dr. de Bock worked at GE Research as Principal Engineer ThermoSciences and platform lead Power-Thermal Mechanical Systems. Dr. de Bock is the former chair of ASME K-16 committee on Heat Transfer in Electronics equipment, ASME Fellow, AIAA member, and holds 50+ patents and publications. Dr. de Bock received his Ph.D. in Mechanical Engineering from the University of Cincinnati and holds MSc degrees from University of Twente in the Netherlands, and University of Warwick in the United Kingdom.

**Presentation Title:** ARPA-E COOLERCHIPS Technology for a Future of Energy Efficient High Power Density/AI Data Centers

**Abstract:** The Department of Energy (DOE) Advanced Research Projects Agency – Energy (ARPA-E) was founded to support high-risk/high-reward technologies that could lead to transformational impact in the energy space. The $42M COOLERCHIPS program supports teams to develop a new generation of transformational, highly efficient, and reliable cooling technologies for data centers. The target for COOLERCHIPS is to reduce total cooling energy TUE to less than 5% of a typical data center's IT load at any time and any U.S. location for future high-density compute systems for Enterprise, AI and High-Performance Computing. Technologies supported include broad technical teams pursuing transformational concepts in single-phase, two-phase, immersion and passive cooling methods. COOLERCHIPS technologies will achieve these goals by dramatically reducing the thermal resistance of heat rejection to R<0.01 K/W through diverse approaches, which will allow for coolants to exist at temperatures much closer to operating temperatures of the latest generation of chips (targeting <10°C difference between chip and coolant for >1 kW chipsets). This will result in more efficient heat removal from the facility. The program will develop solutions for systems of >80 kW/m3, equivalent to about >3 kW per server or 126 kW/42U rack and modular data centers with >20 kW/m3 or about >1 MW per 40ISO container. In addition, there is an emphasis to develop new tools and methods for component and system reliability engineering to ensure that data center system uptime similar to existing air-cooled data centers today, 99.982% tier 3 can be maintained. An overview of the program, technology approaches and impact paths will be presented.

**THURSDAY, OCTOBER 10**
8:00 AM–9:30 AM
CALIFORNIA BALLROOM DE, MEZZANINE LEVEL

**Ani Natekar**
*Technical Sourcing Manager*
*Meta Platform Inc.*
*Fremont, California*

**Ani Natekar** currently serves as technical sourcing manager at Meta where is responsible for a techno-commercial roadmap through the end of the decade. Ani has been instrumental in driving Meta's journey towards liquid cooling by predicting changes in technology ahead of the curve, developing metrics and development criterion to evaluate these technological changes and enabling a stable supply chain to support the execution of these technological changes into our data centers. Over the past few years, this has involved setting a vision for a new supply chain catering to performance, sustainability and operability and incorporated explorations around chiller plants, natural refrigerants, various liquid to liquid and liquid to air heat exchanger systems and supply chain developments of these commodities. Ani stays curious around liquid cooling optionality, industry adoption of technologies beyond the now ubiquitous single phase cold plate, high performance and sustainable fluids and explorations in advanced packaging. Prior to joining Meta, Ani spent ~15 year in the industrial and automotive space leading engineering, product development, marketing, general management, and business development teams. Notably, the last ~6 years where he sold into the data center industry. Experiencing growth within the hyperscale industry for about a decade, Ani was able to bring the growth mindset to Meta's supply chain drafting our first supplier partnership program and helping move our sourcing efforts from commodity sourcing to strategic supply chain management.

**Presentation Title:** Data Center Industry's Supply Chain Readiness and Scalability for Liquid Cooling

**Abstract:** Over the past couple of years, the industry has significantly improved our understanding of AI/ML module and rack power estimations and the datacenters needed to support this new performance envelope. Until a few short years ago, supply chains for liquid cooling and 1000W TDP/ GPU were thought to be a problem we might need to address by the end of the decade. Over the past couple of years, we started exploring how to deal with those levels of heat rejection and evaluating if the technologies we are developing today can address these heat rejections. By last year, we were building data centers and setting up supply chains to accommodate heat rejections well above those thresholds. To accommodate for these high heat rejection demands, the industry, including Meta, had to transition away from a decade long history of air-cooled data centers and introduce liquid to the rack. Given the extensive footprint of air-cooled data centers in the world and the times it takes to design and build a new liquid cooled datacenter, the industry has had to develop solutions that can cater to high performance compute in both infrastructure applications.

At Meta, we strive to develop a stable supply chain for our data center infrastructure that will account for the technological advancements needed for our high-performance needs and deliver on Meta's corporate sustainability targets while maintaining our abilities to efficiently manage our growing footprint. We are doing this by focusing on three primary drivers: performance, sustainability, and operability. We are also continuously refining and building out our technology pipeline by a combination of work streams around academic institutions, industry affiliations, supplier roadmaps and in-house developments. In this talk, we would like to share how we saw the industry identify key driving factors in a technology shift, down select the appropriate technology and standup stable supply chains in a limited vendor landscape to enable the industry pivot to liquid cooling.

# Track 4

**WEDNESDAY, OCTOBER 9**
8:00 AM–9:30 AM
CALIFORNIA BALLROOM DE, MEZZANINE LEVEL

**Professor John Thome**
**Prof. Emeritus EPFL,**
Technical Director of JJ Cooling Innovation
Lausanne, Switzerland

**John Thome** is Prof. Emeritus EPFL, Technical Director of JJ Cooling Innovation in Lausanne, Switzerland and Chairman of ALPEMA (aluminum brased plate heat exchangers manufacturers association). He is a co-founder of JJ Cooling since 2018 and previously held the chair of Professor of Heat transfer at the EPFL while as well heading the Doctoral Program in Energy (over 100 PhD students). He received his Ph.D. at Oxford University and is the author of 5 books and is the Editor-in-Chief of the 16-volume Encyclopedia of Two-Phase Heat Transfer and Flow. He received the 2017 Nusselt-Reynolds Prize, the IEEE 2019 Richard Chu ITHERM Award, the ASME 2019 Allan Kraus Thermal Management Medal and the 2010 ASME Heat Transfer Memorial Award. He is a long-time researcher and technology specialist in microscale and macroscale two-phase heat transfer and two-phase systems, pulsating heat pipes, loop thermsyphons, and refrigeration systems. He is ranked by Google Scholar as 1st, 3rd, and 4th in research citations in Boiling, Two-Phase Flow, and Electronics Cooling, respectively. He has been actively engaged in developing new thermal technologies and simulation tools for the electronics cooling, nuclear power, petrochemical, automotive , refrigeration, and air-conditioning industries.

**Presentation Title:** Passive Two-Phase Cooling of Electronics and Energy Efficiency

**Abstract:** Passive two-phase cooling of electronics has been around with us and progressing for many years, with very widespread use of wicked heat pipes and more recently vapor chambers. Two other passive two-phase devices are emerging strongly now: Loop thermosyphons (LTSs) and Pulsating heat pipes (PHPs. While vertical-pipe thermosyphons (evaporator at bottom and condenser at top in counterflow) have been and still are also widely used, loop thermosyphon cold plates are now emerging in the cooling industry to handle high heat flux applications, in which the working fluid flows up a riser tube from the evaporator to the condenser and then the condensate down through a downcomer tube back to the inlet of the evaporator. LTS technologies are available for the cooling of individual datacenter CPUs as well as cooling of multiple heat sources in Edge micro-datacenters, telecom photonics transmitters and entire high power datacenter racks (including AI). Pulsating heat pipes are the most recent addition to the category of passive cooling technologies, devices which create self-activated and self-induced two-phase flow without any internal wick structure, just a loop microchannel serpentine going back-and-forth from its evaporator zone to its condenser zone. These are gaining industrial traction for cooling of power electronics, 5G base stations, CPUs, etc. The talk will present and describe how LTSs and PHPs function and the keys to their performance and usage. Notably, when utilizing LTSs and PHPs, the thermal efficiency of electronics cooling attains the new goals for reducing electrical cooling power consumption, with PUEs as low as 1.017 and 1.030 in performance tests with air-cooled condensers, and in several cases using natural convection to air from the condenser are able to take the PUE to 1.00, that is zero energy consumption (fan off) that are promising for electronics on standby or low/ medium operation. Numerous examples of actual units/systems for a variety of industries will be described.

# Track 5

**WEDNESDAY, OCTOBER 9**
8:00 AM–9:30 AM
CALIFORNIA BALLROOM D, MEZZANINE LEVEL

**Adam A. Wilson**
Team Leader, Thermal Sciences and Engineering Team
Energy Sciences Division, United States Army Combat Capabilities Development Command Army Research Laboratory

**Adam A. Wilson** leads the Thermal Sciences and Engineering Team at the Army Research Laboratory in Adelphi, MD, and serves as Program Manager for a multidisciplinary team of researchers across Army, Navy, and Air Force, and chairs the Interagency Advanced Power Group's Electrical Materials Panel. He earned his B.S. degree in Physics and B.A. in Mathematics from University of Northern Iowa and his Ph.D. in Engineering Physics from Rensselaer Polytechnic Institute. Adam's research in developing novel nanoscale thermal metrology techniques led him to Madrid, Spain as part of the NSF International Research Experience program, and then to the Army Research

Laboratory for a postdoctoral appointment that has subsequently morphed into a career in federal civilian service researching thermal energy conversion, mitigation, and storage. He has received several honors and awards, such as ARL's Technically Bold Award, multiple Best Paper Awards at IEEE ITherm, and Northern Iowa's Purple and Old Gold Award.

**Presentation Title**: Size and Timescale Matching for Transient-Aware Thermal Management

**Abstract:** Over the last decade, compact and extreme-environment thermal management has made large strides. Conventional thermal management approaches aim to minimize thermal resistance to the surroundings in order to keep temperature fluctuations due to varying heat loads below some critical temperature (which varies by the application). However, in an attempt to simplify and multifunctionalize components in the interest of reducing size, weight, and power (SWaP) required to meet operational goals, transient responses to heat loads may bring failure to bear sooner. In this talk, I will discuss key considerations when designing thermal management solutions for heavily SWaP-constrained platforms, and some recent demonstrations of these efforts coming out of our work at the Army Research Laboratory. Germane to these efforts are incorporation of phase-change enthalpy to extend thermal time constant when nearing a critical temperature. I will cover recent work in this area (both ours and others') and will highlight recent trends across the micro- and nanoscale heat transfer community that provide insights into efficiently designing transient-aware thermal management solutions.

# Track 6

**THURSDAY, OCTOBER 10**
1:30 PM–2:15 PM
CALIFORNIA BALLROOM, SALON D

**Sheng Xu**
UC San Diego
San Diego, CA

**Sheng Xu** is a Professor and Jacobs Faculty Scholar at UC San Diego. He earned his B.S. degree in Chemistry from Peking University and his Ph.D. in Materials Science and Engineering from the Georgia Institute of Technology. Subsequently, he pursued postdoctoral studies at the Materials Research Laboratory at the University of Illinois at Urbana-Champaign. His research group is interested in developing new materials and fabrication methods for soft electronics, with a particular focus on wearable ultrasound technology. His research has been presented to the United States Congress as a testimony to the importance and impact of funding from the National Institutes of Health. He has received numerous honors, including the NIH Maximizing Investigators' Research Award, NIH Trailblazer Award, Sloan Fellowship, IEEE EMBS Technical Achievement Award, ETH Zürich Materials Research Prize for Young Investigators, MRS Outstanding Early Career Investigator Award, and a finalist of the Blavatnik National Awards for Young Scientists. He is an AIMBE Fellow.

**Presentation Title:** Wearable Ultrasound Technology

**Abstract:** The use of wearable electronic devices that can acquire vital signs from the human body noninvasively and continuously is a significant trend for healthcare. The combination of materials design and advanced microfabrication techniques enables the integration of various components and devices onto a wearable platform, resulting in functional systems with minimal limitations on the human body. Physiological signals from deep tissues are particularly valuable as they have a stronger and faster correlation with the internal events within the body compared to signals obtained from the surface of the skin. In this presentation, I will demonstrate a soft ultrasonic technology that can noninvasively and continuously acquire dynamic information about deep tissues and central organs. I will also showcase examples of this technology's use in recording blood pressure and flow waveforms in central vessels, monitoring cardiac chamber activities, and measuring core body temperatures. The soft ultrasonic technology presented represents a platform with vast potential for applications in consumer electronics, defense medicine, and clinical practices.

The advent of soft ultrasonic technology represents a convergence of interdisciplinary expertise, combining principles from materials science, engineering, and medical research. At its core, this technology leverages flexible and biocompatible materials, meticulously engineered to interface seamlessly with the human body. Advanced microfabrication techniques further enhance its capabilities, enabling the integration of sophisticated components onto wearable platforms with unprecedented precision and reliability. One of the key strengths of soft ultrasonic technology lies in its ability to penetrate deep tissues, capturing physiological signals with unparalleled fidelity. Unlike conventional surface measurements, which may be susceptible to environmental factors and external interference, signals acquired from deep tissues offer a direct window into the body's internal dynamics. This deeper insight enables more accurate assessments of vital parameters such as blood pressure, cardiac function, and core body temperature, facilitating earlier detection of abnormalities and proactive intervention.

Moreover, the noninvasive nature of soft ultrasonic technology ensures patient comfort and compliance, eliminating the need for invasive procedures or cumbersome monitoring equipment. This aspect is particularly crucial in clinical settings, where continuous monitoring of patients, especially those with chronic conditions, is paramount. By seamlessly integrating into everyday life, wearable devices powered by soft ultrasonic technology empower individuals to take charge of their health, fostering a culture of proactive wellness management.

Beyond healthcare, the versatility of soft ultrasonic technology extends into diverse fields, ranging from sports performance monitoring to military applications. In sports medicine, for instance, real-time assessment of athletes' physiological responses during training and competition can inform personalized training regimens and injury prevention strategies. Similarly, in military settings, wearable devices equipped with soft ultrasonic sensors offer invaluable insights into soldiers' health and performance in demanding operational environments, enhancing mission readiness and troop welfare.

As research and development in soft ultrasonic technology continue to advance, the horizon of possibilities expands even further. From enhanced diagnostics and therapeutic interventions to personalized healthcare solutions tailored to individual needs, the potential for positive impact is boundless. By bridging the gap between technological innovation and human health, soft ultrasonic technology epitomizes the transformative power of interdisciplinary collaboration, paving the way for a future where healthcare is not just reactive but proactive, preventive, and personalized. In essence, the journey of soft ultrasonic technology represents a testament to human ingenuity and a beacon of hope for a healthier, more connected world. As we navigate the complexities of modern healthcare, it serves as a reminder that the most profound solutions often emerge at the intersection of science, technology, and compassion.

**TUESDAY, OCTOBER 8**
9:30AM –10:45AM
CALIFORNIA BALLROOM, SALON A

**Workshop 1: Status, Challenges, and Opportunities in Electronics Packaging from a Government/Lab Perspective**

**Date:** October 10, 9:30 – 10:45 a.m. Pacific Time

**Location:** California-Salon-M, Holiday Inn San Jose – Silicon Valley

**Chair/Moderator:** Sreekant Narumanchi, U.S. Department of Energy (DOE) National Renewable Energy Laboratory (NREL)

**Speakers:** Mark Spector (U.S. Office of Naval Research - ONR), Benjamin Leever (U.S. Air Force Research Laboratory - AFRL), Mike Fish (U.S. Army Research Laboratory - ARL), Sreekant Narumanchi (U.S. DOE NREL)

**Abstract:** Each speaker will get up to 10 minutes (including introduction by the Chair and transitions) to talk about the status, challenges, and opportunities in electronics packaging of interest to their agency/office/lab, and to pose a list of key questions for the audience. The intent will be to open this up to the audience for about 35 minutes for feedback, Q&A and discussions.

**Dr. Mark S. Spector** is a Program Officer in the Sea Warfare and Weapons Department at the Office of Naval Research where he manages research in thermal science, metamaterials, energy conversion, and climate resilience. In addition, he sits on the Steering Committee of the Department of Defense Energy and Power Community of Interest, the US Navy Climate Working Group, and the NATO Applied Vehicle Technology Power and Propulsion Systems Technical Committee. Previously, he worked as a Research Physicist at the Naval Research Laboratory. He received his doctorate in Physics from the Massachusetts Institute of Technology and bachelor's degrees in physics and applied mathematics from the University of California at Berkeley.

**Abstract:** Thermal Challenges for Future Military Platforms: Modern land, sea, and air warfare technologies are trending towards significantly higher power loads with transient behavior that present unique challenges in thermal system design. Traditional design approaches assume steady state operation and rely on overdesign to meet worst-case scenarios. Moreover, advanced control techniques are virtually absent in most thermal systems. Therefore, tremendous opportunities exist to reduce the size, weight and power consumed by thermal management systems associated with these loads through the development of innovative electronic packaging approaches, the design of energy-efficient system architectures that utilize advanced control strategies, and their effective integration onto military platforms.

**Dr. Benjamin Leever** is currently the Chief of the Polymers & Specialty Materials Branch in the Air Force Research Laboratory (AFRL) Materials & Manufacturing Directorate. Dr. Leever leads a team of approximately 100 government, military, and contractor personnel, managing an annual budget of ~$40M. In this role, he contributes to the development of next-generation technologies to deliver capabilities to the U.S. Air Force (USAF) and U.S. Space Force (USSF) related to survivability in contested and extreme environments. Prior to this current role, Dr. Leever served the Manufacturing & Industrial Technologies division as the Technical Director. He also served as Government Chief Technology Officer of NextFlex, a $200M public-private partnership established to create a domestic manufacturing ecosystem in flexible hybrid electronics. Earlier in his career, Dr. Leever served as the Advanced Development Leader for AFRL's Soft Materials Branch, leading an external portfolio focused on flexible electronics and biomaterials. He has also previously led a research team focused on the development and modeling of multifunctional materials for structural power applications. Dr. Leever earned a B.S. in Chemical Engineering from the University of Cincinnati and a Ph.D. in Materials Science and Engineering from Northwestern University.

**Abstract:** Electronics processes, components, and packaging for extreme environments:

The USAF and USSF need electronic systems that can survive extreme hot and cold temperatures, large temperature swings, high vibrations, and other harsh conditions. This presentation will highlight materials and process innovations as well as ongoing challenges in AFRL's work to expand the operating window of electronic devices and packaging in extreme environments.

**Dr. Michael Fish** leads the transient thermal program as part of the Power Integration and Architectures Branch at the U.S. Army Research Laboratory. He has expertise in embedded thermal management, simulation, and thermal test bed development. His current effort is in the packaging and management of highly transient electronic systems, with particular focus on directed energy weapons and vehicle electrification and power conversion. He holds a Ph.D. in Mechanical Engineering from the University of Maryland, College Park where he studied thermal phenomena in heterogeneously integrated electronic systems. He received his B.S. and M.S. from the University of Virginia, studying micro/nanoscale heat transport and thermal metrology.

**Abstract:** The electrified burden on Army platforms and soldiers has been and will continue to dramatically increase as next-generation sensors, edge computing, and electronic and directed energy warfare mature and are deployed to future theaters. From an operational energy perspective, this means electronics and their packages must do more with less: higher output or throughput – often under extreme conditions – while minimizing size and weight. To accomplish this will require engineering beyond the edge of currently available design trade spaces, made possible by both advances in materials as well as a mission-aware reconceptualization of how components in a package interoperate with each other and systems they are embedded in to maximize effectiveness.

**Dr. Sreekant Narumanchi** is a Distinguished Member of Research Staff and Manager of the Advanced Power Electronics and Electric Machines group within the Center of Integrated Mobility Sciences at the National Renewable Energy Laboratory, where he has completed almost 20 years. He leads a Group of 17 researchers focused on packaging, thermal management and reliability of power electronics and electric machines for electric-drive vehicles and multiple other applications. His group has collaborated with over 80 institutions cutting across industry, universities, national and research labs, and federal agencies. Sreekant is an American Society of Mechanical Engineers (ASME) Fellow, and recipient of the 2023 ASME Avram Bar-Cohen Memorial Medal and the 2022 THERMI Award. He has over 120 peer-reviewed publications and 5 patents. Sreekant had/has multiple leadership roles in conferences, journals, committees, and advisory boards. He received a Ph.D. from Carnegie Mellon University (2003), M.S. from Washington State University (1999), and B. Tech. from Indian Institute of Technology Kanpur (1997), all in Mechanical Engineering.

**Abstract:** Advanced Power Electronics and Electric Machines Packaging, Thermal Management, and Reliability for Electric-Drive Vehicles: Electronics, power electronics, and electric machines are becoming important for an array of mobility/transportation, renewable energy, and energy efficiency applications. I will describe some metrics, challenges, and opportunities for power electronics, electric machines, and electric traction-drive systems for light-, medium-, and heavy-duty vehicle applications. After that, I will give a brief overview of my group's research activities in power electronics, electric machines and integrated (electric) traction-drive systems. This includes thermal management, thermomechanical reliability, state-of-health monitoring, and power module design, development, fabrication, and characterization aspects. I will conclude with some key questions for the audience pertaining to opportunities and research and development pathways.

**Workshop 2: K-16 Mentorship Workshop**

**Date:** October 8, 3:50 – 5:15 p.m. Pacific Time

**Location:** California-Salon-K, Holiday Inn San Jose – Silicon Valley

**Chair/Moderator:** Tiwei Wei, Purdue University; Xiangyu Li, University of Tennessee Knoxville; Ronald J Warzoha, United States Naval Academy.

**Speakers/Mentors:** Bidzina Kekelia, National Renewable Energy Laboratory (NREL); Soloman Adera, University of Michigan; Prabhakar Subrahmanyam, Intel

**Dr. Tiwei Wei** is an Assistant Professor at Purdue University's School of Mechanical Engineering. Prior to his role at Purdue, he completed a postdoctoral research tenure in Stanford University's NanoHeat lab between 2020 and 2022. He received his Ph.D. degree in the 3D system integration department at Interuniversity Microelectronics Centre (imec) and KU Leuven, Belgium in 2020, focusing on developing electronic cooling solutions for high-performance 3D systems. Before that, he held senior research positions at Tsinghua University and Hong Kong University of Science and Technology from 2011 to 2015, delving into advanced microelectronic packaging techniques. His current research emphasis encompasses advanced semiconductor packaging and heterogeneous integration, spanning processing, materials, architecture development, chip-package interactions, reliability, and efficient thermal management technologies. He authored over 60 scientific publications in leading journals, conference proceedings, and authored over 10 patents. Dr. Wei actively contributes to the academic community, serving as a session chair and member of the technical program committee in various electronic packaging conferences like IEEE ESTC, REPP, 3DIC, SHTC, Itherm and EPTC. Additionally, he has held leadership roles such as vice-chair of IEEE Electronic Packaging Society (EPS) Silicon Valley Chapter and currently the founder and chair of IEEE EPS Central Indiana Chapter. He received the 2020 IMEC Ph.D. Excellence Award and the 2024 Intel's Rising Star Faculty Award.

**Dr. Xiangyu Li** is an assistant professor at the Department of Mechanical, Aerospace, and Biomedical Engineering at the University of Tennessee Knoxville. His research focuses on thermal management in buildings and electronics to enhance energy efficiency. Key areas of his work include the design of high-temperature heat exchangers, water adsorption for atmospheric water harvesting and thermal energy storage, and solar desalination.

Prior to this appointment, he received his Ph.D. degree from Purdue University with Prof. Xiulin Ruan and worked as a postdoctoral associate at MIT with Prof. Evelyn Wang. He is the author of 22 peer reviewed journal papers and holds three US and international patents. His work on radiative cooling paint is awarded as The Best Inventions of 2023 by TIME magazine and holds the Guinness World's Record as the World's Whitest Paint.

**Dr. Ronald Warzoha** is currently an Associate Professor at the United States Naval Academy. Prior to his tenure at USNA, he served as a team lead for the Transformational Computing Thermal Management team at Northrop

Grumman. He also spent a brief time at the Johns Hopkins Applied Physics Lab as a Senior Scientist, where his focus was on the development of novel shape memory alloy-based thermal storage materials and thermal camouflage systems. In his role at the USNA, he was awarded the Apgar Award for Teaching Excellence, given to one junior faculty member every two years. His research work recently earned him the ASME EPPD Early Career Engineer Award, and he is an Associate Editor for the ASME Journal of Electronic Packaging and the ASME Journal of Open Engineering. Dr. Warzoha has over 40 peer-reviewed journal articles, two patents, and has received major funding from the Office of Naval Research, the Joint Technologies Office, NRO, the Defense University Research Instrumentation Program. His work is presently funded by the National Institute of Standards and Technology (NIST) through the United States CHIPS Act.

**Dr. Bidzina Kekelia's** professional experience in engineering spans over 30 years and he has large number of publications on thermal management and clean energy technologies. Currently he is a Senior Research Engineer in the Advanced Power Electronics and Electric Machines (APEEM) Group within the Center of Integrated Mobility Sciences at the National Renewable Energy Laboratory (NREL). Since joining NREL in 2015, Bidzina's research efforts are focused on vehicle thermal management, exploring novel cooling methods for power electronics, and traction drives for ground electric vehicles (EV) and electrified aviation. Before coming to NREL, he was a postdoctoral research associate at the University of Utah, working on development of a thermal battery prototype for cabin climate control in electric vehicles.

Bidzina has also worked in the power generation and energy sector. Under the auspices of the U.S. Agency for International Development, he provided technical expertise and advisory support to the Ministry of Energy of Georgia. Bidzina developed a power generation dispatch optimization model to identify the export capacity of existing and proposed electricity production facilities in the country, prepared pre-feasibility techno-economic studies for attracting funding to major power sector projects, including high-voltage transmission line, hydropower plants, and provided consulting services and engineering oversight on several power sector-related rehabilitation projects.

Bidzina earned his Bachelor's (Hons) in Mechanical Engineering from Georgian Technical University (1992), M.S. in Renewable Energy (Solar Thermal & PV) from the University of Oldenburg (1999) and Ph.D. in Mechanical Engineering from the University of Utah (2012).

**Dr. Solomon Adera** is an Assistant Professor in the Mechanical Engineering Department at the University of Michigan. He received his MS and PhD from the Massachusetts Institute of Technology in 2012 and 2016, respectively. From 2016-2019, he was a postdoctoral researcher at the School of Engineering and Applied Sciences at Harvard University. His research interests include fundamental studies of micro/nanoscale heat and mass transfer, thermal management, fog/water harvesting, and solar-thermal energy systems. Solomon was the recipient of the National Science Foundation Graduate Research Fellowship Program from 2010-2013.

**Dr. Prabhakar Subrahmanyam** is a Senior Technical Lead and Senior Staff Principal Thermal Engineer at Intel, renowned for his expertise in thermal management from devices to data centers. He specializes in cooling at the silicon and package levels for post-silicon validation and broader strategies across the silicon chip ecosystem, including client, desktop, server, and AI silicon. Notably, he served as the chief validation thermal architect for the Ponte Vecchio chip, Intel's first exascale GPU chip, which powers the Aurora supercomputer at the U.S. Argonne National Laboratory.

Dr. Prabhakar holds a PhD and Masters in Aerospace Engineering, with a focus on reentry heat transfer, as well as a first Masters in Computer Science and a Bachelors degree in Physics. He has authored over 60 papers and holds more than 50 patents in thermal management. His contributions have earned him 5 AIAA Best Paper Awards, 3 IEEE Best Paper Awards, and a gold medal for the best thesis.

In addition to his work at Intel, Dr. Prabhakar is a Visiting Professor at SRM University in India, where he established a lab for electronic cooling and teaches a Capstone program in Electronic Cooling, pioneering an industry internship within the classroom environment for undergraduate students.

**Workshop 3: Reliability of Additively Manufacturing Flexible and Stretchable Electronics – Experiments, Models, and Applications**

**Date:** October 8, 9:30 – 10:45 a.m. Pacific Time

**Location:** California-Salon-A, Holiday Inn San Jose – Silicon Valley

**Co-Chairs:** Nicholas Ginga, UAHuntsville; Rui Chen, Eastern Michigan University

**Dr. Nick Ginga** is an Assistant Professor in Mechanical and Aerospace Engineering at the University of Alabama in Huntsville. He obtained his Master's and PhD degrees in Mechanical Engineering from Georgia Tech and has held postdoctoral research positions at The University of Michigan and Georgia Tech in both Mechanical Engineering and Biomedical Engineering. His research lab has interests that include mechanical testing and finite element modeling of flexible electronics and electronic packaging, thin film fracture mechanics, fabrication and characterization of nano/microstructures and devices, and the interface of nano/micro fabrication and biosystems.

**Abstract:** Reliability Evaluation of Additively Manufactured Stretchable Electronics: Research in the field of flexible and stretchable electronics has grown rapidly in recent years due to their applications in the fields of biomedical engineering, wearable electronics, consumer electronics, and the defense industry. The diverse materials used in stretchable electronics require different mechanical test requirements for their development compared to rigid electronics in order to replicate the unique multidirectional loadings that they experience during their use. This presentation will discuss the different classifications of flexible and stretchable electronics, the various materials and applications that are being used and investigated to create devices, specific methods that have been developed to test their mechanical reliability, and the mechanical modeling approaches to simulate their behavior while subjected to these unique loading scenarios.

**Dr. Rui Chen** is currently an Assistant Professor in the School of Engineering, Eastern Michigan University, specializing in Mechanical Engineering. She joined EMU in Fall 2023. Prior to this role, she was a Postdoctoral Fellow at the George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology, from 2021 to 2023. Her research has been focused on design and modeling, fabrication, characterization, reliability assessment, and failure analysis of flexible electronics. Over the past six years, her interdisciplinary work has resulted in 19 journal and conference publications. Additionally, she is an active member of the Institute of Electrical and Electronics Engineers (IEEE), the Society of Women Engineers (SWE), and the American Society of Mechanical Engineers (ASME). She has been elected to serve as a member of the Thermal/Mechanical Simulation and Characterization Committee (TMSC) of the Electronic Components and Technology Conference (ECTC) of the Institute of Electrical and Electronics Engineers (IEEE). Dr. Chen received her Ph.D. degree in Mechanical Engineering from the Georgia Institute of Technology in 2021, her MS degree in Mechanics from the University of Chinese Academy of Sciences in 2015, and her BS degree in Engineering Mechanics from the Shanghai Jiao Tong University in 2012.

**Abstract:** Reliability Assessment of Additively Manufactured Flexible Electronics Under Bending: Flexible electronics, increasingly prevalent in wearable devices, soft robotics, and other advanced technologies, face significant reliability challenges under geometric deformations. While stretching is a common deformation these products may experience, bending presents more issues due to the more complex stress and strain distributions involved. This presentation will explore the specific challenges of maintaining the reliability of flexible electronics under bending conditions, including an overview of current challenges and methods used to assess reliability. It will cover the complexities introduced by bending, the associated failure modes, and methods for evaluating reliability, including experimental techniques, numerical simulations, and machine learning approaches. Additionally, the presentation will discuss future research directions aimed at addressing these challenges, such as developing more sophisticated modeling approaches to better capture the intricate electrical and mechanical relationships under bending and investigating novel materials and fabrication techniques to enhance reliability.

**Workshop 4:** Advancing Electronics Packaging and Heterogeneous Integration: Insights from InterPACK 2024 Panels, Tutorials and Workshops

**Date:** October 9, 11:00 a.m. – 12:15 p.m. Pacific Time

**Location:** California-Salon-K, Holiday Inn San Jose – Silicon Valley

**Chair:** Gamal Refai-Ahmed, AMD

**Speakers:**

**Abstract:** A special panel on "Silicon/Packaging Technology Development to Enable the Next Generation of AI," where distinguished executive leaders from industry and academia will explore the forefront of advancements revolutionizing AI hardware. This panel will reveal an exciting deep dive into the latest silicon and packaging innovations, examining how these technologies are transforming AI performance and efficiency. The expert panelists will unravel the complexities of advanced packaging techniques like 2.5D and 3D stacking, highlighting their critical role in overcoming challenges related to heat dissipation and signal integrity. Discover the importance of heterogeneous integration, the cutting-edge thermal management solutions, and the evolving role of materials science in semiconductor packaging. Engage with insights on how the industry is addressing higher interconnect density demands, the potential of silicon photonics, and the strategies balancing performance, power consumption, and cost in AI chip packaging. Additionally, the panel will explore the implications of a potential advancements, the role of machine learning in packaging optimization, and the significance of academia-industry collaboration in pushing technological boundaries. This panel is set to ignite audience curiosity and provide a comprehensive overview of the emerging technologies poised to disrupt the AI hardware landscape in the coming years. Don't miss this opportunity to gain invaluable knowledge and foresight from the leaders driving the future of AI technology.

**Dr. Gamal Refai-Ahmed**

**Dr. Pushkar P. Apte** serves as Strategic Technology Advisor and leads the Global Data & Artificial Intelligence (AI) Initiative at SEMI, the electronics industry consortium representing 3300+ companies worldwide. His work focuses on two exciting opportunities at the intersection of semiconductors and AI–innovative, system-level solutions to accelerate innovation in AI, and digital twins to improve efficiency of semiconductor research & development, design and manufacturing.

Dr. Apte received his Master's and Ph.D. degrees from Stanford University in Materials Science and Electrical Engineering, and his Bachelor's degree in Ceramic Engineering from the Indian Institute of Technology, Varanasi, India. Dr. Apte also holds an Executive M.B.A. from Southern Methodist University.

Until June 2024, Dr. Apte served as Director of Strategic Initiatives at the University of California, Berkeley, where he built industry-academic partnerships to create intelligent technology solutions for challenging business and societal applications. Previously, Dr. Apte has worked with Texas Instruments Incorporated on cutting-edge research and technology development for semiconductors, with McKinsey & Company as their Global Semiconductor Business Expert, and with the Semiconductor Industry Association as Vice President of Technology. Dr. Apte has served on the Executive Boards of the Semiconductor Research Corporation, International SEMATECH, and the International Technology Roadmap for Semiconductors.

Dr. Apte has over 50 publications and presentations in prestigious international journals, conferences, and institutions, including several Invited Papers. He has received the Norman Hackerman Young Author Award from the Electrochemical Society for Best Paper in the Journal of the Electrochemical Society, and the Graduate Student Award from the Materials Research Society for Outstanding Research Performance. Dr. Apte also holds 2 U.S. Patents.

**Dr. Bahgat Sammakia** is the vice president for research at Binghamton University and director of the NSF-IUCRC on Energy Smart Electronic Systems (ES2) and Binghamton University's Small Scale Systems Integration and Packaging Center ($S^3IP$), a New York State Center of Excellence. He is a professor of mechanical engineering in the Thomas J. Watson School of Engineering and Applied Science.

Dr. Sammakia has spent much of his research career working to improve thermal management strategies in electronic packaging systems at multiple scales ranging from devices to entire Data Centers.

Dr. Sammakia joined the faculty of the Watson School in 1998 following a fourteen-year career at IBM where he worked in the area of research and development of organic electronic systems. He has contributed to several books on natural convection heat transfer and is also the principal investigator or co-principal investigator on several cross-disciplinary research projects.

Dr. Sammakia earned his bachelor's degree in mechanical engineering from the University of Alexandria, Egypt, and his master's and doctorate in mechanical engineering from the State University of New York at Buffalo. He was a post-doctoral fellow at the University of Pennsylvania. Dr. Sammakia has over 200 published papers in refereed journals and conference proceedings, has contributed to several books in the areas of heat transfer and electronics packaging. He also holds 18 US patents and 12 IBM technical disclosures in the area of electronics packaging. Dr. Sammakia was the General Chair for the ITherm 2006 conference and the Interpack 2012 Conference. Dr. Sammakia is a Fellow of both the IEEE and the ASME and is the editor of the Journal of Electronic Packaging, Transactions of the ASME and an associate editor of the CPMT Transactions of the IEEE.

**Dr. Suresh Ramalingam** is a Corporate Fellow at AMD, where he leads the Advanced Packaging & Thermo-Mechanical Technologies sector. With a Ph.D. and M.S. in Chemical Engineering from MIT, and a B.Tech from IIT Madras, his extensive education has laid the foundation for over two decades of significant contributions in the semiconductor industry. Dr. Ramalingam's career began at Intel Corporation, where from 1994 to 2000, he developed advanced interconnect technologies and managed optical materials engineering. As a co-founder and Director of Materials at Scion Photonics from 2000 to 2002, he pioneered fiber-optic technologies until its acquisition by JDS Uniphase, where he then served as Senior Engineering Manager until 2004. His tenure at Xilinx from 2004 to 2022 saw him spearheading advanced packaging solutions for FPGAs, impacting 28nm technology developments significantly. Since 2022, at AMD, he focuses on enhancing silicon performance through innovative packaging and reliability improvements. Dr. Ramalingam has been recognized with numerous awards, including the ECTC 2011 Outstanding Session Paper and multiple keynote honors at prestigious IEEE conferences and other technical symposia worldwide, reflecting his leadership in integrating academic insights with industry applications to drive forward next-generation semiconductor technologies.

**Dr. Pradeep Lall** is the MacFarlane Endowed Distinguished Professor and Alumni Professor with the Samuel Ginn College of Engineering and Director of the Auburn University Electronics Research Institute. He holds Joint Courtesy Appointments in the Department of Electrical and Computer Engineering and the Department of Finance. He is a member of the technical council and academic co-lead of automotive and asset monitoring TWGs of NextFlex Manufacturing Institute. He is the author and co-author of 2-books, 15 book chapters, and over 975 journal and conference papers in the field of semiconductor packaging, electronics reliability, manufacturing, safety, testing, energy efficiency, and survivability. Dr. Lall is a fellow of the ASME, a fellow of the IEEE, a fellow of the NextFlex National Manufacturing Institute, and a fellow of the Alabama Academy of Science. He is recipient of the SEMI R&D Achievements Award for landmark contributions to Additive Printed Electronics, ASME Avram Bar-Cohen Memorial Medal, IEEE Biedenbach Outstanding Engineering Educator Award, Auburn University Research Advisory Board's Advancement of Research and Scholarship Achievement Award, IEEE Sustained Outstanding Technical Contributions Award, NSF-IUCRC Association's Alex Schwarzkopf Award, Alabama Academy of Science Wright A, Gardner Award, IEEE Exceptional Technical Achievement Award, ASME-EPPD Applied Mechanics Award, SMTA's Member of Technical Distinction Award, Auburn University's Creative Research and Scholarship Award, SEC Faculty Achievement Award, Samuel Ginn College of Engineering Senior Faculty Research Award, Three-Motorola Outstanding Innovation Awards, Five-Motorola Engineering Awards, and over Fifty Best-Paper Awards at national and international conferences. Dr. Lall has served in several distinguished roles at the national and international level including serving as a member of the National Academies Committee on Electronic Vehicle Controls, Member of the IEEE Reliability Society AdCom, IEEE Reliability Society Representative on the IEEE-USA Government Relations Council for R&D Policy, Chair of Congress Steering Committee for the ASME Congress, Member of the technical committee of the European Simulation Conference EuroSIME, Associate Editor for the IEEE Access Journal, and Associate Editor for the IEEE Transactions on Components and Packaging Technologies. Dr. Lall is the founding faculty advisor for the SMTA student chapter at Auburn University and a member of the editorial advisory board for SMTA Journal. He received the M.S. and Ph.D. degrees in Mechanical Engineering from the

University of Maryland and the M.B.A. from the Kellogg School of Management at Northwestern University.

**Workshop 5: Women in Engineering**

**Date:** October 8, 3:50 – 5:15 p.m. Pacific Time

**Location:** California-Salon-A, Holiday Inn San Jose – Silicon Valley

**Moderator:** Priyanka Dobriyal, AccessAI

**Speakers/Mentors:** Narmadha Parhasarthy, Tensetorrent; Rui Chen, Eastern Michigan Univ.; John D. Williams, Boeing,

**Biography:** Dr. Priyanka Dobriyal is the founder/CEO of non-profit AccessAI under 5013c which aims to provide AI education free of cost. She has a very diverse technical experience from Intel most recently as a TA/Chief of Staff in Memory IO group in DCAI. Priyanka joined Intel in 2009 as a Process Engineer after completing her Ph. D from the University of Massachusetts, Amherst in the area of Polymer Physics. She has a MS in Chemistry from Indian Institute of Technology Roorkee. Priyanka is known in the industry for innovations through her publications (>10 Intel and external), technical and non-technical conference presentations and advocating for a diverse and an inclusive culture. She has 9 approved patent filings. In her spare time, Priyanka balances her fast-paced career with dedicated and heart-felt community service by organizing STEM outreach events.

**Biography:** Dr. Rui Chen is currently an Assistant Professor in the School of Engineering, Eastern Michigan University, specializing in Mechanical Engineering. She joined EMU in Fall 2023. Prior to this role, she was a Postdoctoral Fellow at the George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology, from 2021 to 2023. Her research has been focused on design and modeling, fabrication, characterization, reliability assessment, and failure analysis of flexible electronics. Over the past six years, her interdisciplinary work has resulted in 19 journal and conference publications. Additionally, she is an active member of the Institute of Electrical and Electronics Engineers (IEEE), the Society of Women Engineers (SWE), and the American Society of Mechanical Engineers (ASME). She has been elected to serve as a member of the Thermal/Mechanical Simulation and Characterization Committee (TMSC) of the Electronic Components and Technology Conference (ECTC) of the Institute of Electrical and Electronics Engineers (IEEE). Dr. Chen received her Ph.D. degree in Mechanical Engineering from the Georgia Institute of Technology in 2021, her MS degree in Mechanics from the University of Chinese Academy of Sciences in 2015, and her BS degree in Engineering Mechanics from the Shanghai Jiao Tong University in 2012.

**TUESDAY, OCTOBER 8**
1:30 PM–2:15 PM
CALIFORNIA BALLROOM, SALON E

**Tutorial Chair/Co-Chairs:** Victor Chiriac, Raffaele Luca Amalfi and John D. Williams

**Tutorial 1: Liquid Cooling and Heat Reuse Technologies**

**Title:** Chasing Hotspots via Jet Vector Impingement – A dynamic hotspot mitigation method in high power density Silicon

**Abstract:** High power density silicon, particularly with non-uniform power distribution, presents significant challenges in thermal management due to the formation of localized hotspots. These hotspots, which vary in location and intensity depending on workload, can severely limit performance and reliability. Direct jet impingement offers superior heat removal capabilities due to high heat transfer coefficients, but traditional implementations lack the ability to dynamically target hotspots. In this talk/presentation, I will explore a patented jet vector impingement technique that actively tracks and cools hotspots in real-time. Case studies involving both bare die silicon and a Xeon multi-chip module will be presented, showcasing the effectiveness of jet vector impingement in reducing peak temperatures and improving overall thermal performance. Pre- and post-impingement temperature data will be analyzed to quantify the benefits of this innovative cooling approach.

**Presenter/Instructor:**
Dr. Prabhakar Subrahmanyam
Intel

**Dr. Prabhakar Subrahmanyam** is a Senior Technical Lead and Senior Staff Principal Thermal Engineer at Intel, renowned for his expertise in thermal management from devices to data centers. He specializes in cooling at the silicon and package levels for post-silicon validation and broader strategies across the silicon chip ecosystem, including client, desktop, server, and AI silicon. Notably, he served as the chief validation thermal architect for the Ponte Vecchio chip, Intel's first exascale GPU chip, which powers the Aurora supercomputer at the U.S. Argonne National Laboratory. Dr. Prabhakar holds a PhD and Masters in Aerospace Engineering, with a focus on reentry heat transfer, as well as a first Masters in Computer Science and a Bachelors degree in Physics. He has authored over 60 papers and holds more than 50 patents in thermal management. His contributions have earned him 5 AIAA Best Paper Awards, 3 IEEE Best Paper Awards, and a gold medal for the best thesis. In addition to his work at Intel, Dr. Prabhakar is a Visiting Professor at SRM University in India, where he established a lab for electronic cooling and teaches a Capstone program in Electronic Cooling, pioneering an industry internship within the classroom environment for undergraduate students.

**Title:** Modeling Energy Efficient Two-Phase Heat Transfer System

**Abstract:** Exponential growth of AI workloads is driving the need for high performance chip packages that cannot be thermally managed by energy- and water-intensive chilled air-cooling solutions implemented in Data Centers today. A two-phase heat transfer system, that utilizes the liquid to vapor phase conversion of a working fluid for transferring the heat to the ambient environment, can provide energy-efficient thermal management of high-performance AI systems while eliminating water consumption and maintaining system reliability in any geographical location. This short tutorial will describe the exemplar computationally manageable high-fidelity components- as well as system-level models that are necessary for the assessment and development of such a cooling system.

**Presenter/Instructor:**
Dr. Pritish R. Parida
IBM

**Dr. Pritish Parida** is a Senior Research Scientist at IBM Research. He is currently the co-PI of IBM-ARPA-E program on Systems Two-phase cooling (DE-AR0001577). He has extensive experience in the development of cutting-edge thermal technologies including chip-embedded two-phase cooling, for high performance computing systems and embedded applications such as UAVs (unmanned aerial vehicles), RF (radio frequency), and 5G devices. He obtained his Ph.D. in Mechanical Engineering from Virginia Tech. Dr. Parida has received several technical and innovation awards at IBM as well as outside including Outstanding Technical Achievement Award (2016, 2021, 2022), Outstanding Research Award (2021), Research Division Award (2012, 2016, 2021), Outstanding Technical Paper Award (2012), Best Paper Award (SEMI-Therm 2017), Best Poster Award (GOMACTech 2017). Dr. Parida has co-authored over 60 peer-reviewed publications, three book chapters, and holds over 100 issued patents.

**Tutorial 2: AI/ML and Industry Trends**

**Title:** Scaling Prospects of Machine Learning Compute Resources through Light

**Abstract:** This course provides an in-depth exploration of the tools, technologies, and strategies that are advancing the scaling of compute fabrics to vastly expand machine learning capabilities through photonics. It delves into how photonics can revolutionize machine learning implementations within the CMOS ecosystem, with a particular emphasis on enhancing interconnection density in system-in-package (SiP) designs. As the industry increasingly focuses on co-packaged optics as a key strategic direction, understanding the complexities of this technology is crucial. The capabilities and functionalities of co-packaged optics will significantly impact the benefits they can deliver to the broader CMOS ecosystem.

**Presenter/Instructor**
Dr. Amr S. Helmy
University of Toronto

**Dr. Amr S. Helmy** is a professor in the department of electrical and computer engineering at the University of Toronto. Prior to his academic career, Amr held a position at Agilent Technologies - UK, between 2000 and 2004. At Agilent his responsibilities included developing lasers and monolithically integrated optoelectronic circuits. He received his Ph.D. and M.Sc. from the University of Glasgow with a focus on photonic integration technologies, in 1999 and 1995 respectively. His research interests include photonic device physics, with emphasis on plasmonic nanostructures, nonlinear and quantum photonics addressing applications in information processing / sensing, and data communications. Amr is an active volunteer and leader of the IEEE Photonics Society, currently serving as an Elected Member of the Society's Board of Governors and as a Distinguished Lecturer. He was also the recipient of the Society's 2019 Distinguished Service Award.

**Tutorial 3: Efficient Energy Systems**

**Title**: Sustainable Data Centers: Low GWP Refrigerant Transition

**Abstract:** The rapid expansion of data center capacity and increasing power densities to meet growing computing needs will result in a significant surge in electricity demand for cooling. The increasing emphasis on sustainability in the industry is prompting efforts to improve the energy efficiency of air-cooled data centers, utilize more effective direct-to-chip two-phase cooling technologies, and transfer large amounts of heat to the district heating network. Selecting the right refrigerant is crucial for maximizing performance and minimizing the environmental impact of heat transfer systems. Both regulatory actions and corporate sustainability goals are driving a major transition towards using low global warming potential (GWP) refrigerants in the data center industry. This transition marks a significant advancement in environmental responsibility within the industry. The presentation will delve into the regulations surrounding refrigerants, key refrigerant attributes for different heat transfer systems, and the existing low-GWP refrigerant options, particularly hydrofluoroolefins (HFOs). It will evaluate the benefits, challenges, and opportunities associated with transitioning to low-GWP refrigerants. The presentation will review the atmospheric chemistry of specific HFOs and their environmental impact.

**Presenter/Instructor**:
Dr. Nitin Karwa
Honeywell

**Dr. Nitin Karwa** currently works as the Principal R&D Engineer at Honeywell's Buffalo Research Labs. In this role, he focuses on developing new heat transfer fluids for various applications such as electronic cooling, air conditioning, and industrial heat pumps. Dr. Karwa holds a PhD in Mechanical Engineering from the Technical University of Darmstadt in Germany and has spent 3 years on postdoctoral research at universities in Germany and Australia. With 11 years of industry experience, he specializes in vapor compression systems for HVAC and industrial heating, and two-phase heat transfer systems for electronics cooling. Additionally, he has authored over 25 articles in peer-reviewed international journals and conferences on heat transfer and energy systems, making significant contributions to the academic community.

**Title:** Thermal Management for Electric Vehicles: Batteries and Power Electronics

**Abstract:** Heat transfer is a limiting factor in the reliability and performance of next-generation batteries and power electronics for electric vehicles (EVs). While researchers focus on optimizing device performance to improve, for example, battery capacity (driving range), thermal effects have often been relegated to a secondary concern. But overheating batteries are a major topic of concern as they have caused fires across a range of systems, and overheating power electronics degrade the system reliability. Further, electric vehicles, being mobile platforms, have limited heat dissipation pathways, exacerbating thermal challenges. This talk will discuss two key thermal management challenges: (1) effective thermal management of battery systems (including the multi-physics coupling of heat transfer, electrochemistry, mechanics, and fluid dynamics within thermal management systems) and (2) improving reliability of power electronics through novel architectures that incorporate phase change material-based thermal buffers to reduce temperature spikes throughout the driving cycle. Ultimately, thermal informed design of batteries and power electronics can lead to more efficient, reliable, and safe electric vehicles.

**Presenter/Instructor:**
Dr. Amy Marconnet
Purdue University

**Amy Marconnet** is a professor of Mechanical Engineering and professor of Materials Engineering (by Courtesy), as well as a Perry Academic Excellence Scholar, at Purdue University. She received a B.S. in Mechanical Engineering from the University of Wisconsin – Madison in 2007, and an M.S. and a PhD in Mechanical Engineering at Stanford University in 2009 and 2012, respectively. Her dissertation focused on thermal phenomena in nanostructured materials. She then worked briefly as a postdoctoral associate at the Massachusetts Institute of Technology, before joining the faculty at Purdue University in August 2013. Her work has won outstanding paper awards at ITherm 2012, InterPACK 2017, ITherm 2019, ITherm 2023, and ITherm 2024. In 2017, she won the Woman in Engineering Award from the ASME Electronics & Photonics Packaging Division (EPPD). In 2020, she won the Bergles-Rohsenow Young Investigator Award in Heat Transfer and the Outstanding Graduate Student Mentor from the Official Mechanical Engineering Graduate Association (OMEGA) and the College of Engineering. She won a Humboldt Fellowship for Experienced Researchers and conducted research at Karlsruhe Institute of Technology in the 2021-22 academic year.

**Tutorial 4:** Additive Manufacturing for Electronic Devices and Interconnects

**Title:** Additive Manufacturing of Electronic Devices and Interconnects

**Abstract:** Additive manufacturing of electronic devices and interconnects continues to advance with the evolution of new printing methods and associated conductive and dielectric material inks. This tutorial will review printing methods, materials, and applications. The ability to print smaller circuit features, ground planes, filled vias and printed "wire bonds" that interconnect the substrate to silicon devices will be described. Recent results from studies on medical and industrial sensors, printed RF components, high-temperature electronics, and high-power wide- bandgap SiC power electronics packages will be included.

**Presenter/Instructor:**
Dr. Mark D. Poliks
Binghamton University

**Mark D. Poliks** is a SUNY Distinguished Professor and Empire Innovation Professor of Materials Science and Engineering and Systems Science and Industrial Engineering at the Thomas J. Watson College of Engineering and Applied Science, Binghamton University, State University of New York. He is the founding director of the Center for Advanced Microelectronics Manufacturing (CAMM), a New York State Center of Advanced Technology and home to the New York Node of the federally supported NextFlex Manufacturing USA. Poliks has made sustained contributions to the fields of materials processing, electronics packaging, flexible, hybrid and additive electronics that are relevant to a variety of medical and industrial applications. Poliks was the General Chair of the 69th IEEE Electronic Components and Technology Conference (ECTC). He is a Fellow of NextFlex, an elected member of the IEEE Electronics Packaging Society (EPS) Board of Governors, serves as the director of student programs and is an IEEE Distinguished Lecturer.

# Panel Sessions

**TUESDAY, OCTOBER 8**
11:00AM–12:15PM
CALIFORNIA BALLROOM, SALON A

**Scientific Panel Title:** Thermal, Mechanical, and Electrical Challenges in Advanced Mobile, Wireless, AI, IoT, Automotive, and High-Power Computing Devices

**Panel Moderator:** Dr. Victor Chiriac (CEO, Global Cooling Technology Group, LLC)

**Bio:** ASME Fellow, CEO and Managing Director of Global Cooling Technology Group, LLC. Held technology/engineering leadership roles, led corporate thermal technology teams and roadmaps, worked on leading-edge wireless technologies with Motorola (1999-2010), Qualcomm (2010 – 2018) and Futurewei (2018 – 2019). Elected Chair of the ASME K-16 Electronics Cooling Committee in 2015 and the Arizona and New Mexico IMAPS (International Microelectronics and Packaging Society) Chapter President in 2010. Co-editor of Electronics Cooling Magazine since 2016 and leading member of the organizing committees of ASME/InterPack, IMECE and IEEE/ITherm. 25 U.S. and International issued patents, 2 US Trade Secrets, 1 US Defensive Publication and 117 papers in scientific journals and at conferences. Recipient of the ASME K-16 Clock award in 2018 for "scientific contributions and leadership in promoting best thermal management of electronics engineering practices". Diamond Innovation and Technology Leadership Awards at Qualcomm in 2016-2017, and the Corporate Award for Technology Innovation at Motorola in 2002. PhD (1999) in Aerospace and Mechanical Engineering, University of Arizona, Tucson, USA.

**Panel Abstract:** The digital era demands higher performance, increased data processing, and faster processors. Heterogeneous computing, which includes CPUs, GPUs, high-speed interconnects, and other elements, is driving advancements in the industry. The rise of 5G/6G technologies is accelerating mobile communication, AI, and IoT, creating infrastructure for vast amounts of data and fostering smarter, more connected environments. This panel will explore the future of thermal management in electronics and address advanced system-level thermal, mechanical, and electrical challenges, as well as technical and business solutions.

**Confirmed Panelists:**

**Panelist 1:** Eric Bert (President, Exentis AG USA)
**Panelist 2**: Herman Chu (Senior Principal, Celestica, USA)
**Panelist 3**: Ali Heydari (Technical Director, NVIDIA, USA)
**Panelist 4:** Rozalia Beica (Chief Marketing Officer, LQDX, USA)
**Panelist 5**: Russell Kempt (VP of New Business Development, Diamond Foundries, USA)
**Panelist 6:** Ross Q. Smith (CEO, RADX Technologies, USA)

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**Eric Bert** (President, Exentis AG USA)

**Bio:** Eric Bert holds a BSME from UMass-Amherst and has a 30+ year track record in disruptive manufacturing technology introduction and management. Eric currently serves as President of Exentis North America and is responsible for building a North American beachhead for Switzerland based Exentis Group AG. Prior roles in Additive Manufacturing included; SVP Commercial at Inkbit, COO at 3DMEDiTech, SVP Global Sales at ARCAM (a GE Additive company), and SVP at Stratasys North America during its high growth period. Earlier, Eric held technology and management positions in the high-volume printed circuit and electronics assembly sectors. He further completed expat assignments in Thailand and Australia starting-up, building, and operating large-scale manufacturing operations.

**Presentation Title:** Additive Screen Printing: Industrialized AM Technology for Production of Parts with Ultra-Fine Features and Structures Using a Wide Range of Materials

**Presentation Abstract:** Additive Screen Printing is a new approach to sinter based additive manufacturing for volume mass production of industrial parts. Using conventional screen-printing techniques combined with high-speed precision optics and industrial handling automation, Exentis has introduced a new, unique technology platform that enables cost-effective, mass production of industrial parts with ultra-fine features and structures using a wide range of metals, ceramics, and other materials. This presentation will outline how the technology works, its capabilities compared to conventional production technologies like; PM, MIM/CIM, and other additive techniques, as well as outline serval thermal management cooling structure part applications where Exentis' capability to produce very small holes, thin walls, and clean, complex micro-channels, using highly thermally conductive materials, delivered successful results. More information on Exentis can be found at www.exentis-group.com

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**Herman Chu** (Senior Principal, Celestica, USA)

**Bio:** Herman Chu is a Senior Principal Engineer at Celestica and manages the thermal engineering team in North America. His passion, since early 2000, has been in energy efficiency and sustainability for telco space and data centers. He established rack level power density design targets for networking equipment design based upon different parameters, such as global energy consumption and data center cooling performance and efficiency, before the term "Green" was coined for sustainability. He was an early participant in the Telecom industry in defining the metrics for measuring energy efficiency for telco equipment. Throughout his career, he has been an industry leader in pioneering efforts developing and deploying high performance thermal solutions, such as high-fin density folded/zipper fin heat sink, heat pipe, vapor chamber and pumped-2-phase liquid cooling for commercial computing/networking equipment

**Presentation Title:** Challenges with Direct Immersion Cooling

**Presentation Abstract:** Impacts with material compatibility, hardware design constraints, safety and compliance, as well as serviceability will be reviewed.

**Russell Kempt (Vice President, Diamond Foundry, USA)**

**Bio:** Russell Kempt is a seasoned tech sales and marketing executive with nearly 30 years of experience in Silicon Valley. With a proven track record of building and leading successful revenue growth from early startup phase to IPO. He is currently a Vice President of Worldwide Sales and Marketing for Diamond Foundries, USA His expertise in developing and executing go-to-market strategies, building customer relationships, and driving revenue growth has made him a valuable asset to numerous tech companies throughout his career.

**Presentation Title:** Single Crystal Diamond (SCD), the ultimate thermal management solution Presentation Abstract: Single crystal diamond (SCD), with its exceptional thermal conductivity, electrical insulation and other unique properties, emerges as the ultimate thermal management solution for advanced AI chips and high-power electronics. Its superior heat dissipation capabilities can significantly enhance the performance, efficiency, and reliability of these devices. This abstract explores the potential of diamond-based thermal management solutions, highlighting its advantages over traditional materials and discussing the challenges and future opportunities in this field.

**Dr. Ali Heydari (Technical Director, NVIDIA, USA)**

**Bio:** Ali Heydari is Distinguished engineer and Data Center Technologist at Nvidia in charge of all data center cooling technology development. He is developing direct to chip liquid cooling technologies using cold plates, cooling distribution units and manifolds for Nvidia's high heat density data centers. Prior to Nvidia, he worked as senior director in charge of Rigetti's Quantum Computers using the most futuristic technology in today's data center compute. Prior to that he served as Senior Technical Director and Chief Data Center Architect at Baidu, the largest search engine and AI company in China. He was server and data center architect in charge of hardware and data center design, development and deployment in China's largest data center search and AI company. Formerly, he was Senior Hardware Engineer at Twitter where he was responsible for grounds up development of Twitter's data center ODM server development. Earlier, he was Senior Hardware Engineer at Facebook where he helped in developing Facebook's original OCP server and data center products. Prior to that he worked at Sun Microsystems and spend about 10 years as Associate Professor of Mechanical Engineering at Sharif University of Technology in Iran. He received his B.S. in mechanical engineering from University of Illinois, Urbana, M.S., Ph.D. in mechanical engineering and M.A. in applied mathematics from University of California, Berkeley. He has over 25 issued patents in data center cooling technologies.

**Presentation Title:** Not available yet. Please provide
**Presentation Abstract:** Not available. Please provide

**Rozalia Beica, Field Chief Technology Officer, Rapidus, USA**

**Bio:** Rozalia Beica is a distinguished leader in the Semiconductor and Advanced Packaging industry, with more than 25 years of experience. Her expertise encompasses a unique mix of broad cross-industry expertise, including electronic materials, substrates, equipment, device & system manufacturing, and market intelligence. She held senior positions at industry leading companies, including AT&S, DuPont, Yole Developpement, Lam Research and Applied Materials. She recently joined Rapidus, as Field CTO, focusing on Packaging Technologies. An active participant in industry activities, Rozalia led numerous symposiums globally, consortia activities, technical working groups and industry roadmaps activities. Rozalia served on the advisory board of IEEE EPS, IMAPS and 3DinCites, and currently she is a member of the Advisory Board at IMPACT and Terecircuits. Rozalia's academic achievements include a M.Sc. in Chemical Engineering from Polytechnic University Timisoara, a M.Sc. in Management of Technology from KWU, and a Global Executive MBA from Instituto de Empresa.

**Presentation Title:** From Chips to Systems: How Advanced Packaging is Empowering AI and High-Performance Computing

**Presentation Abstract:** In the rapidly evolving landscape of Artificial Intelligence (AI) and High-Performance Computing (HPC), heterogeneous integration and advanced packaging have emerged as a critical enabler of innovation. This presentation will provide an overview of the industry trends and applications that will continue to drive the growth of the semiconductor and advanced packaging market. It will look at the AI & HPC impact on the future growth of our industry and the unprecedented market inflection it drives along with the challenges it brings and the innovation required to address them. The evolution of advanced packaging and interconnect technologies will be presented highlighting their pivotal role as a foundational element addressing the needs of AI, chiplet and heterogeneous integration.

**Ross Q. Smith**, CEO, RADX Technologies

**Bio:** Ross Q. Smith is a seasoned high-tech executive with over 30 years of technical and business experience that includes executive management, fund raising, M&A, marketing, business development, engineering management and innovation. With a solid history in founding and leading successful, high-tech startup companies and orchestrating business-unit turnarounds, Ross has demonstrated success in growing businesses from concept to market-leadership positions. Smith is a recognized expert in general management, team building, technical marketing and product development in the areas of consumer electronics, fabless semiconductors, mission critical and real-time embedded and safety critical systems and software, Commercial-Off-the-Shelf (COTS) products, 2D/3D graphics, GPGPU, parallel and high-performance computing, video game technology, renewable energy and precision metrology systems and instrumentation. Smith's portfolio of prior experience includes co-founder, executive and technical management, and key contributor roles at 3dfx, Quantum3D and RADX Technologies, and executive and/or senior management roles at Bruker Nanosurfaces, Soft Machines, Rapport, GarretCom, Media Vision, Pellucid, Jigsaw Informatics, Alchemy Power, Silicon Graphics, MIPS Technologies, Tracor, Atlantic Research and Ford Aerospace

**Presentation Title:** Putting 10 Lbs. in a 5 Lb. Bag - the Power and Cooling Challenges of Standardized Form Factor COTS Products

**Presentation Abstract:** Standardized Form Factor Systems are a mainstay of the COTS Electronics Market: integrators and OEMs combine multiple, disparate functional modules to provide a given system level capability. Examples of popular Standardized Form Factors for backplane, slot and board level specifications include PCIe, PXIe, CPCIe, ATCA, MicroATCA, OpenVPX, SOSA, etc. With these standards, add-in-cards or modules must fit into specific envelopes for Size, Available Power and Available Cooling. Specific examples and challenges will be discussed for PXIe, a popular standard for modular test and measurement.

**Panel session 2**

**Panel Title:** Additive Manufacturing for Domestic Electronics Packaging

**Panel Moderator:** Dr. Janos Veres (NextFlex)

**Bio:** Janos Veres is Director of Hybrid Electronics Strategy at NextFlex, the US Institute of Flexible Hybrid Electronics Manufacturing Innovation. He is a seasoned technologist, with over 30 years' experience in printed, flexible, hybrid electronics and related fields, successfully driving multimillion dollar revenue programs with major electronics, automotive, chemical and consumer product companies. Janos has held R&D, manufacturing and management positions at PARC, PolyPhotonix, Kodak, Merck, Avecia, Zeneca and Gestetner, where he developed printed circuits, electronic materials, OLEDs, displays, medical devices as well as novel process technologies. He brings experience of industrial partnerships and joint development projects in the US, Europe and Asia. Janos holds a Ph.D. in Solid State Electronics from Imperial College, London. He is author of over 65 patents.

**Panel Abstract:** There is a growing interest in US Industry and Government to revitalize the growth of Advanced Packaging in the US. Packaging is not only a necessary element of semiconductor manufacturing, but it is viewed as a growth engine to augment Moore's Law in the era when miniaturization of chip features is becoming increasingly challenging. The importance of packaging has been recognized by the CHIPS Program and numerous international forums. As the US is seeking to close the gap with Asia in semiconductors manufacturing, it is essential to renew a domestic supply chain and infrastructure. US industrial partnerships and consortia are actively looking for ways to create access to domestic packaging. A number of US industrial, academic and government pioneers have been investigating additive electronics technologies as a potential solution. We invited several of them to this panel to discuss their vision and the progress they see in additive packaging. Additive technologies have the potential to jumpstart manufacturing based on lower capital investment. These emerging technologies can scale rapidly with need, providing a distributed manufacturing footprint. Importantly, additive manufacturing connects scales and can support "scaling down, scaling out and scaling up" articulated by the National Advanced Packaging Manufacturing Program (NAPMP). Our panel represents a broad cross-section of the US supply chain, with in-depth experience in manufacturing innovation and partnerships. Our guests will discuss packaging as part of the bigger picture of domestic electronics manufacturing; the integration from silicon to chiplets, heterogeneous 3D packages, circuit boards all the way to entire systems.

**Panelists:**

Professor Pradeep Lall, MacFarlane Endowed Distinguished Professor, Alumni Professor, and Director, Auburn University
Christopher Tabor, Air Force Research Laboratory
Andras Vass-Varai, Siemens
Dr. Adam Scotch, Brewer Science
Dr. Dan Gamota, NextFlex

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**Prof. Pradeep Lall, Auburn**

**Bio:** Pradeep Lall is the MacFarlane Endowed Distinguished Professor and an Alumni Professor with the Department of Mechanical Engineering. He is Director of the NSF-CAVE3 Electronics Research Center at Auburn University. He holds Joint Courtesy Appointments in the Department of Electrical and Computer Engineering and the Department of Finance. He is a member of the technical council and academic co-lead of automotive and asset monitoring TWGs of NextFlex Manufacturing Institute. He is the author and co-author of 2-books, 15 book chapters, and over 900 journal and conference papers in the field of electronics reliability, manufacturing, safety, test, energy efficiency, and survivability. Dr. Lall is a fellow of the ASME, fellow of the IEEE, a Fellow of NextFlex Manufacturing Institute, and a Fellow of the Alabama Academy of Science. He is recipient of the IEEE Biedenbach Outstanding Engineering Educator Award, Auburn University Research Advisory Board's Advancement of Research and Scholarship Achievement Award, IEEE Sustained Outstanding Technical Contributions Award, NSF-IUCRC Association's Alex Schwarzkopf Award, Alabama Academy of Science Wright A, Gardner Award, IEEE Exceptional Technical Achievement Award, ASME-EPPD Applied Mechanics Award, SMTA's Member of Technical Distinction Award, Auburn University's Creative Research and Scholarship Award, SEC Faculty Achievement Award, Samuel Ginn College of Engineering Senior Faculty Research Award, Three-Motorola Outstanding Innovation Awards, Five-Motorola Engineering Awards, and over Forty Best-Paper Awards at national and international conferences. Dr. Lall is the founding faculty advisor for SMTA student chapter at Auburn University and member of editorial advisory board for SMTA Journal

**Presentation Title:** Promise of Additive Fabrication Process for Heterogeneous Integration Packaging

**Presentation Abstract:** It is widely realized that future performance gains in electronics will require increased reliance on packaging. Application-specific integration of chips and discrete components will require manufacturing methods that allow for cost-effective manufacturing in lower volumes and reduction or mitigation of the sunk costs required for hard tooling needed for conventional packaging. A number of additive methods have emerged for the fabrication of substrates, including aerosol-jet, inkjet, direct-write, gravure offset, extrusion-print, and screen-print. The adoption of additive methods provides additional benefits in the form of lower material waste, reduction or elimination of hard tooling, shorter production ramp-up, smaller lot sizes, and higher customization.

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**Christopher Tabor, Air Force Research Laboratory**

**Dr. Christopher Tabo**r is a Research Lead within the Materials and Manufacturing Directorate at the Air Force Research Laboratory (AFRL). After graduating with a Ph.D. in chemistry from Georgia Tech in 2009, he joined AFRL first as a National Research Council Fellow performing research on plasmonic nanoparticle enhancement of organic photovoltaics and then as a staff scientist researching flexible and stretchable electronics, with an emphasis on room temperature liquid metals. Dr. Tabor's work has been highlighted in the defense technology media on multiple occasions and he has published over 60 peer-reviewed journal articles in the area of optical and electronic properties of metals with 16 patents. He currently leads the Polymer and Responsive Materials and Process Research Team, exploring fundamental and early applied research on soft sensors and electronics, responsive structures, and resilient polymers.

**Presentation Title:** Printed Liquid Electronics for Ultra-Soft Stretchable Electronics

**Presentation Abstract:** Liquid metals utilizing low melting point alloys have been increasingly explored over the last decade as an alternative solution to solid conductors where the need to withstand extreme mechanical stress is required. The unique mix of high conductivity and extremely low modulus (on par with human tissue) have made them a target for exploration and prototyping. There has been some fascinating work through the academic literature whereby liquid metal is utilized in a variety of emerging embodiments such as fibers, microcapsules, and interconnects(1). In order to fully embrace this new material set however, the processing of these materials needs to become more routine and reliable while utilizing established techniques. This talk will detail the work that has been done between AFRL and some important collaborators in creating a new generation of liquid metal inks, ELMNT Inks(2), that can be utilized in screen printing, jet printing, and blade coating to allow rapid scale-up of textile based electronics, soft robotic circuitry, and dry electrodes for long term physiological monitoring.

Several applications have been identified wherein ELMNT Inks could fill a specific technical gap in the flexible and wearable electronics communities. Liquid metal inks have been integrated into a variety of textile components to demonstrate resistive heating in areas that require high dexterity such as the hands and feet. Additionally, they are currently being tested as a direct-to-skin dry electrode to monitor a variety of electrophysiology data(3), including EEG, ECG, and EMG, while also being able to provide direct stimulation for muscular therapy and recovery. Thirdly, cabling for data transmission and communication have been demonstrated for use in soft robotics and elastic cabling.

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**Dr. Andras Vass-Varnai (Siemens)**

**Bio:** Dr. Andras Vass-Varnai obtained his MSc and PhD degrees in Electrical Engineering from the Budapest University of Technology and Economics. He spent over a decade at Mentor Graphics as a product manager, leading various R&D projects focused on thermal test hardware and methodologies. Before assuming his current role as a 3D IC reliability solution engineer, Andras served as a business development lead in South Korea and the United States. Now based in Chicago, IL, he is dedicated to contributing to the development of a novel 3D IC package toolchain, leveraging his experience in thermal and reliability engineering. His main areas of interest include thermal management of electronic systems, advanced applications of thermal transient testing and modeling, semiconductor packaging, characterization of TIM materials, and reliability testing of semiconductor devices.

**Presentation Title:** Novel EDA Toolkits as Enablers for High-Density Advanced Packaging

**Presentation Abstract:** As semiconductor companies navigate growing design complexity and the need for enhanced computational power, advanced packaging techniques like 2.5D/3D designs have become essential. In the panel we will explore the integration of novel EDA toolkits that facilitate combined design and multiphysics simulation, addressing the need for cohesive toolchains and breaking down silos among engineering disciplines to support advanced semiconductor package design.'.

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**Dr. Adam Scotch (Brewer Science)**

**Bio:** Dr. Adam Scotch has been Director of R&D, Smart Devices and Printed Electronics at Brewer Science in Springfield, MO for the last 3.5 years. He is responsible for the technical direction of environmental sensors development as well as materials R&D for additively manufactured electronics. Prior to joining Brewer Science, Adam was Director of Manufacturing at antenna tech start-up Wafer for 3.5 years, responsible for product development, engineering, scale to manufacturing, and general operations. Adam held various technical leadership roles over 13 years in R&D at lighting company OSRAM, and lead the company's efforts in printed electronics. His expertise is in materials science, process development, LED devices, and packaging. Prior to OSRAM, he was a National Research Council Postdoctoral Fellow at the National Institute of Standards and Technology (NIST). He holds 25 U.S. Patents and 9 refereed journal publications. Adam has a B.S. and Ph.D. in Materials Science and Engineering from Lehigh University, Bethlehem, PA.

**Presentation Title:** Building Circuits from the Ground Up: Materials Innovation for Additive Electronics Presentation Abstract: As the electronics industry faces new challenges in miniaturization and performance, there is a critical need for innovative materials and processes to drive the next wave of growth. Traditional microelectronics technologies, from photolithography to PCB fabrication, have remained largely unchanged for decades. While additive manufacturing has seen rapid development, primarily on polymers and metals for structural applications, there is a significant opportunity to advance materials specifically for electronics, such as low-loss dielectrics materials for high-frequency applications.

Brewer Science is at the forefront of this innovation, leveraging its extensive expertise in polymer chemistry to develop printable, low-loss dielectric materials that meet the needs of modern electronics. These materials have the potential to revolutionize domestic electronics packaging by enabling new capabilities, reducing costs, and supporting a more resilient domestic supply chain. Additive manufacturing will enable more freedom for integrated and innovative design approaches, such as creating complex 3D traces and vias, and embedded functions like RF and optical waveguides, all within a single manufacturing process. This holistic method allows for the construction of electronic circuits from the ground up, breaking down traditional silos by merging the function of chips, packages, and PCBs into unified multifunctional components.

As the U.S seeks to close the gap with global competitors and build a robust domestic infrastructure, additive manufacturing offers a pathway to achieving these goals. With a strong foundation in material science and a commitment to advancing additive electronics, Brewer Science is poised to lead the charge for disruptive change in the electronics industry, just as it did with bottom antireflective coatings 40 years ago.

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**Dr. Daniel Gamota, NextFlex**

**Bio:** Dr. Daniel Gamota has over 25 years of experience in the electronics manufacturing industry, spanning SEMI, middle end of line (MEOL), backend of the line (BEOL), outsourced semiconductor assembly and test (OSAT), and surface mount technology (SMT) operations at an Original Equipment Manufacturer (OEM) and an Electronic Manufacturing Services (EMS) provider.

He has been a principal investigator (PI) for several microelectronics programs awarded by the Defense Advanced Research Projects Agency (DARPA) and the National Institute of Standards and Technology's Advanced Technology Program (NIST ATP). Also, he is active in and has chaired committees for developing microelectronics guidelines, standards, and roadmaps by the Institute of Electrical and Electronics Engineers (IEEE), the International Electronics Manufacturing Initiative (iNEMI), and IPC.

Dr. Gamota is currently the Executive Director of NextFlex. Prior to NextFlex, he was the Vice President of the Manufacturing and Innovation Organization, Global Operations at Jabil Inc. and was the director and fellow of the Technical Staff at Motorola. He was elevated to an IEEE Fellow and was named a Dan Noble Fellow at Motorola for his contributions and leadership in microelectronics design, materials, packaging, processes, assembly, and testing. He earned a Ph.D. in engineering from the University of Michigan and a Master of Business Administration from the Kellogg School of Management at Northwestern University.

**Presentation Title:** Establishing an Ecosystem for Advanced Microelectronics Packaging

**Presentation Abstract:** The pace of innovation by members of the advanced microelectronics packaging ecosystem is poised for accelerated growth due to the support from the National Advanced Packaging Manufacturing Program (NAPMP). This growth will foster unparalleled advancements in designs, materials, additive processes, assembly equipment, and testing platforms for innovative advanced packaging architectures. Several trends are impacting the ecosystem as it experiences an increase in demand for the introduction of microelectronics packaging that offer solutions to address challenges in several high growth markets e.g., Networking & Telecommunications, Healthcare, Cloud, Compute & Storage, Industrial & Energy, Automotive & Transportation, Defense & Aerospace, and Smart Home & Appliances. The innovators of advanced microelectronics packaging are leveraging a portfolio of capabilities typically seen at Semiconductor Back End Of Line (BEOL), Outsourced Semiconductor Assembly and Test (OSAT), and Printed Circuit Board Assembly (PCBA) services providers to establish a resilient domestic supply chain. Members of the advanced microelectronics packaging community are establishing a microelectronics innovation pipeline by implementing a process that stresses "Strategic Versus Tactical – A Deliberate Balance" and emphasizes 1) Collaborating (Open and Pre-competitive), 2) De-risking (Technology, Manufacturing, and Market), and 3) Accelerating & Compressing (Timelines, Workstreams). The microelectronics packaging ecosystem appears to be well positioned to offer product designers with unlimited access to realize their most exciting ideas by providing scalable materials, additive processes, and equipment to build advanced microelectronics packaging.

**Panel session 3**

**Panel Title:** Data center challenges and opportunities

**Panel Moderator**: Dr. Raffaele Luca Amalfi (SEGUENTE Inc.)

**Bio:** Dr. Raffaele Luca Amalfi is the CEO and Co-Founder of SEGUENTE Inc., considered an Innovator, visionary, and industry influencer driving Seguente's strategic business, technology & product roadmap, capital objectives, and growth goals. Prior founding SEGUENTE, he had strategic roles in large corporate companies, leading R&D and commercialization activities in the field of thermal management, and advanced liquid-cooling technologies of high-performance communications and computing systems. He authored over 75 scientific publications in leading journals, conference proceedings, and handbooks, and 20 patents. Dr. Amalfi is the Secretary of the ASME K-16 Heat Transfer Committee, Member of the OCP Heat Reuse Steering Committee, former Guest Editor for the ASME Journal of Electronic Packaging, and recipient of numerous IEEE, ASME and Government Awards.

**Panel Abstract:** Data processing, transport, and storage demands are exponentially increasing, driven by applications in mobile broadband, video/gaming, cloud, 5G networks, Artificial Intelligence, and Internet of Things. Such trends are directly linked to next-generation "digital transformation", which is dominated by intelligent machine-to-machine and human-to-machine communications, automating "everything everywhere" in a new ecosystem. This has profound implications in terms of overall design that mandates greater system functionalities per unit volume, inevitably associated with higher heat densities. Consequently, thermal management using liquid-cooling approaches will be critical to solve increasingly onerous sustainability and performance challenges pressing the large-scale computing and telecommunication systems, which are driving the integration of digital technology into nearly every corner of a society at an unprecedented pace.

**Confirmed Panelists:**

**Panelist 1:** Nicolas Monnier, Staubli
**Panelist 2:** Dr. Amy Marconnet, Purdue University
**Panelist 3:** Dr. Nitin Karwa, Honeywell
**Panelist 4:** Dr. Farnood Rezaie, Cisco

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**Nicolas Monnier (Staubli)**

**Bio:** Nicolas Monnier is the head of business for IT Cooling with Stäubli Fluid Connector Systems in North America. He has been with the company for 19 years previously working as a project manager in R&D for Stäubli in France, where he led the design and the adaptation of fluid connectors for a wide range of demanding industries. Thirteen years ago, he moved to Stäubli's North American headquarters in Duncan, S.C., to provide technical support to the sales network and assist in the development of custom fluid connectors dedicated to special applications. Over the last decade, the use of liquids for thermal management of electronic systems has increased significantly in quantity and also in technical requirements. Nicolas' intrinsic knowledge of fluid connector design positioned him perfectly to address the demanding requests of an industry that requires the highest level of technological innovation and reliability. Nicolas graduated with a M.A.S. in Integrated Product and Process Design from The University of Grenoble (Joseph Fournier University).

**Presentation Title:** The next challenges in thermal management

**Presentation Abstract**: Liquid cooling has become an increasingly popular solution for managing heat in high-performance computing systems, such as super-computer & data centers. While liquid cooling can offer superior thermal performance compared to traditional air-cooled systems, it also poses some challenges as requirements in thermal management are getting higher and higher. This is translated by a need for higher cooling flow rates and therefore find appropriate connection solutions, since the need of the hot swappable system is mandatory. Modularity is becoming a key to quickly adapt installation to the thermal challenges, and quick couplings are a key component of this trend . In parallel to the different developments in liquid cooling, we will discuss some research made with refrigerant fluid , still in line with the increased demand for more thermal efficiency.

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**Dr. Amy Marconnet, Purdue University**

**Bio:** Amy Marconnet is a professor of Mechanical Engineering and professor of Materials Engineering (by Courtesy), as well as a Perry Academic Excellence Scholar, at Purdue University. She received a B.S. in Mechanical Engineering from the University of Wisconsin – Madison in 2007, and an M.S. and a PhD in Mechanical Engineering at Stanford University in 2009 and 2012, respectively. Her dissertation focused on thermal phenomena in nanostructured materials. She then worked briefly as a postdoctoral associate at the Massachusetts Institute of Technology, before joining the faculty at Purdue University in August 2013. Her work has won outstanding paper awards at ITherm 2012, InterPACK 2017, ITherm 2019, ITherm 2023, and ITherm 2024. In 2017, she won the Woman in

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**Dr. Nitin Karwa (Honeywell)**

**Bio:** Dr. Nitin Karwa currently works as the Principal R&D Engineer at Honeywell's Buffalo Research Labs. In this role, he focuses on developing new heat transfer fluids for various applications such as electronic cooling, air conditioning, and industrial heat pumps. Dr. Karwa holds a PhD in Mechanical Engineering from the Technical University of Darmstadt in Germany and has spent 3 years on postdoctoral research at universities in Germany and Australia. With 11 years of industry experience, he specializes in vapor compression systems for HVAC and industrial heating, and two-phase heat transfer systems for electronics cooling. Additionally, he has authored over 25 articles in peer-reviewed international journals and conferences on heat transfer and energy systems, making significant contributions to the academic community.

**Presentation Title:** Not Available at the moment. Please provide
**Presentation Abstract**: Not Available at the moment. Please provide

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**Dr. Farnood Rezaie (Cisco)**

**Bio:** Dr. Farnood is currently a Technical Leader at Cisco Systems Inc. Farnood's expertise is in developing optical networking technologies and silicon photonics-based interconnects. Previously at Tower Semiconductor, Farnood developed industry leading silicon photonics technologies for applications in optical transceivers, A.I. and LiDARs and sensors. Before Tower, Farnood worked on heterogenous integration of III-V materials onto silicon photonics platform. Farnood is chair of IEEE-EPS Photonics technical committee, vice chair of IEEE REPP conference, technical committee member of IEEE OI conference and co-chairs JEDEC Silicon Photonics Qualification and Reliability Standards Task Group (within JC 14.3). Farnood received his PhD from University of Central Florida in 2015.

**Presentation Title:** Not Available at the moment. Please provide
**Presentation Abstract**: Not Available at the moment. Please provide

**Panel session 4**

**Panel Title:** Two-phase Flow for Electronics Cooling

**Panel Moderator:** John Thome, CTO, JJ Cooling and GCTG, ex-EPFL (jothnthomeinc@gmail.com):

**Bio:** John Thome is Prof. Emeritus EPFL, Technical Director of JJ Cooling

Innovation in Lausanne, Switzerland and Chair of ALPEMA (Aluminum Plate Exchangers Manufacturers Association). He received his PhD at Oxford University and is the author of 5 books and Editor-in-Chief of the 16-volume Encyclopedia of Two-Phase Heat Transfer and Flow. He received the 2017 Nusselt-Reynolds Prize, the IEEE 2019 Richard Chu ITHERM Award, the ASME 2019 Allan Kraus Thermal Management Medal and the 2010 ASME Heat Transfer Memorial Award. He is a long-time researcher and technology specialist in microscale and macroscale two-phase heat transfer and two-phase systems, pulsating heat pipes, loop thermosyphons and refrigeration systems. He is ranked by Google Scholar as 1st, 3rd and 4th in citations in Boiling, Two-Phase Flow and Electronics Cooling, respectively.

**Panel Abstract**: Two-phase flow cooling is coming on strong as the new alternative to handle the high AI chip heat loads and well as for mobile electronics, Edge AI compute, 5G base stations, power electronics, EV-aircraft systems, potentially for battery cooling, etc. The choices are principally: 1) pumped two-phase cooling, 2) passive gravity-driven two-phase loop thermosyphons and 3) pulsating heat pipes. Two-phase immersion cooling is also a contender but will not be addressed here. The panelists will present their experiences on laying out new two-phase cooling technologies for their industrial sectors and at looking at the pros-and-cons of two-phase cooling versus water cooling and air-cooling.

**Panel Members (Confirmed):**

Panelist 1: Jean-Philippe (J.P.) Fricker, Chief System Architect at Cerebras Systems
Panelist 2: Dr. Victor Chiriac, CEO and Managing Director of Global Cooling Technology Group
Panelist 3: Dr. Jackson Marcinichen, CEO at JJ Cooling Technology
Panelist 4: Dr. Winston Zhang, CEO of Novark Technologies

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**Jean-Philippe Fricker (Cerebras)**

**Bio:** Jean-Philippe (J.P.) Fricker is Chief System Architect at Cerebras Systems. Before co-founding Cerebras, J.P. was Senior Hardware Architect at rack-scale flash array startup DSSD (acquired by EMC). Prior to DSSD, J.P. was Lead System Architect at SeaMicro where he designed three generations of fabric-based computer systems. Earlier in his career, J.P. was Director of Hardware Engineering at Alcatel-Lucent and Director of Hardware Engineering at Riverstone Networks. He holds an MS in Electrical Engineering from EPFL – École Polytechnique Fédérale de Lausanne, Switzerland, and has authored 42 patents

**Presentation Abstract:** To be received (waiting internal approval).

**Title:** To be received (waiting internal approval).

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**Dr. Victor Chiriac (GCTG)**

**Bio:** ASME Fellow, CEO and Managing Director of Global Cooling Technology Group, LLC. Held technology/engineering leadership roles, led corporate thermal technology teams and roadmaps, worked on leading-edge wireless technologies with Motorola (1999-2010), Qualcomm (2010 - 2018) and Futurewei (2018 - 2019). Elected Chair of the ASME K-16 Electronics Cooling Committee in 2015 and the Arizona and New Mexico IMAPS (International Microelectronics and Packaging Society) Chapter President in 2010. Co-editor of Electronics Cooling Magazine since 2016 and leading member of the organizing committees of ASME/InterPack,IMECE and IEEE/ITherm. 22 U.S. issued patents, 2 US Trade Secrets, 1 US Defensive Publication and 111 papers in scientific journals and at conferences. Recipient of the ASME K-16 Clock award in 2018 for "scientific contributions and leadership in promoting best thermal management of electronics engineering practices". Diamond Innovation and Technology Leadership Award at Qualcomm and the Award for Technology at Motorola. PhD (1999) in Aerospace and Mechanical Engineering, University of Arizona, Tucson, USA.

**Presentation Title:** PHP Cooling for Mobile and Portable Electronics: Challenges and Opportunities

**Presentation Abstract:** The consumer electronics industry develops ever higher performance, more data and faster processors, better graphics processing units (GPUs), high speed interconnects and other elements that push forward the computing performance and user satisfaction. 5G/6G has created a rapid rise in mobile communication and IoT technology, providing the infrastructure needed to carry large amounts of data. All these advancements require much better cooling solutions, especially in thin and compact mobile applications. The presentation will present a breakthrough PHP cooling solution for the mobile industry of the future and beyond.

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**Dr. Jackson Marcinichen (JJ Cooling Technology)**

**Bio:** J.B. Marcinichen is founder and CEO of JJ Cooling Innovation and has over 30 years of experience in HVAC & R systems. He received his PhD in Mechanical Engineering from the Federal University of Santa Catarina, Brazil in 2006. He has authored over 60 scientific and technical papers in indexed journals and international peer-reviewed conferences, book chapters and patents. He is mainly engaged in the development of novel hybrid cooling systems (passive and active) to cool high heat flux electronics using on-chip cooling, pulsating heat pipes and loop thermosyphons. He received the IEEE Best Paper Award at the ITHERM 2020 conference (USA, 2020)

**Presentation Title:** AI High Performance Datacenter and Edge Computers: High Performance Loop Thermosyphon Cooling to 600W and Beyond

**Presentation Abstract:** Passive gravity-driven two-phase thermosyphon cooling technologies have significant advantages over pumped-two-phase flow loops: 1) no pump or energy consumption or electrical connection, 2) cheaper system components, 3) no maintenance of a non-existent pump, driver or power supply, 4) refrigerant charging possible in factory rather than onsite in datacenter, etc. Cooling of new high power AI chips using a thermosyphon is in fact possible by expert designing to attain low flow resistances and thus high flow rates to attain the cooling goals. A new chip level thermosyphon is presented that is capable so far of 600W cooling in a 1U height (900W is contemplated for 2Us and well over 1200W in 3U-4Us). For datacenters without underfloor water cooling, a new air-cooled 2U thermosyphon is presented that has reach > 600W in tests. Edge computing solution is presented for an air-cooled thermosyphon for wall mounting and proven in independent tests, while a new water heat sink cooled thermosyphon for racks is in development within a European project SHIFT2DC.

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**Dr. Winston Zhang (Novark Technologies)**

**Bio:** L. Winston Zhang is the founder and CEO of Novark Technologies based in Shenzhen, China since 2004, and is an adjunct lecturer in the Department of Mechanical Science and Engineering at University of Illinois at Urbana-Champaign since 2022. He has over 35 years of experience in the area of heat transfer and electronics cooling. He received his Ph.D. in mechanical engineering from the University of Illinois at Urbana-Champaign in 1996. He is a licensed professional engineer (P.E.) in the State of Wisconsin, USA and a Fellow of the American Society of Mechanical Engineers (ASME), Asia Liaison for the IEEE Annual Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), Track Co-Chair for the ASME International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems (InterPACK) and a board member of the Taiwan Thermal Management Association (TTMA).

**Presentation Title:** PHPs for Cooling of Power Electronics and 5G Base Stations

**Presentation Abstract:** Air-cooled PHPs will be presented that are ready for industrial use for the cooling of power electronics and 5G base stations. For power electronics, a PHP with Fin Pack will be described that handles significant heat loads and works both with forced air flow (fan) or completely passive natural convection. For 5G, an array of multiple thin plates with embedded PHPs will be described for cooling of electronic boards. Tests results for both applications will be presented and discussed.

**Panel session 5**

**Panel Title:** Machine Learning for Electronics

**Panel Moderator:** Professor Sumanta Acharya, NSF, IIT

**Bio:** Dr. Sumanta Acharya is currently the Program Director of the Thermal Transport Processes (TTP) program at the National Science Foundation (2022-present) and a Professor in the Department of Mechanical, Materials, and Aerospace Engineering at the Illinois Institute of Technology (IIT) in Chicago. From 2016 to 2022 he was also the Chair of Mechanical, Materials, and Aerospace Engineering, IIT Chicago.

Dr. Acharya's primary area of research is in computational and experimental thermal-fluid sciences. He is the author of nearly 500 refereed journal and published conference articles. In recognition of his research, he was awarded the ASME Heat Transfer Memorial Award in the Science category, the AIChE Donald Q Kern Award, and the AIAA Thermophysics Award. Dr. Acharya He was previously the Chair of the ASME Heat Transfer Division. He is a Fellow of the ASME (American Society of Mechanical Engineers) and ASTFE (American Society of Thermal and Fluids Engineers) and Assoc. Fellow of AIAA (American Institute of Aeronautics and Astronautics).

**Panel Abstract:** Modern electronics and data center systems require careful consideration of thermal, electrical and mechanical codesign for optimal performance. There have been significant advances in the last decade on more effective thermal management strategies, materials, components and architectures for improved electrical performance and packaging strategies for higher densities, efficiencies and footprint. Improved simulation methodologies have played an important role for the improved designs. With recent emergence of Machine Learning and data analytics tools, it has become possible to pull together various pieces of data into a neural-net model that can be used for design and can be relied upon from the perspectives of speed and accuracy. In this panel, the various panelists will discuss different approaches for using machine learning for electro-thermal co-design, thermal management, and multi-scale modeling of the disparate length-scale features on a circuit board.

**Confirmed Panelists:**

Panelist 1: Sreekant Narumanchi, Distinguished Member/Manager, National Renewable Energy Lab
Panelist 2: Patrick McCluskey, Professor, Mechanical Engineering, University of Maryland
Panelist 3: Mark Spector, Program Director, Office of Naval Research
Panelist 4: Yoonjin Won, Associate Professor, University of California, Irvine
Panelist 5: Sanghamitra Neogi, Associate Professor, Univ. of Colorado, Boulder
Panelist 6: Connor McCllelan, CEO, DeepSim Inc.

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**Dr. Sreekant Narumanchi**

**Bio**: Sreekant Narumanchi is a Distinguished Member of Research Staff and Manager of the Advanced Power Electronics and Electric Machines group within the Center of Integrated Mobility Sciences at the National Renewable Energy Laboratory, where he has completed almost 20 years. He leads a Group of 17 researchers focused on packaging, thermal management and reliability of power electronics and electric machines for electric-drive vehicles and multiple other applications. His group has collaborated with over 80 institutions cutting across industry, universities, national and research labs, and federal agencies. Sreekant is an American Society of Mechanical Engineers (ASME) Fellow, and recipient of the 2023 ASME Avram Bar-Cohen Memorial Medal and the 2022 THERMI Award. He has over 120 peer-reviewed publications and 5 patents. Sreekant had/has multiple leadership roles in conferences, journals, committees, and advisory boards. He received a Ph.D. from Carnegie Mellon University (2003), M.S. from Washington State University (1999), and B. Tech. from Indian Institute of Technology Kanpur (1997), all in Mechanical Engineering.

**Presentation Title:** Artificial Intelligence/Machine Learning in Power

# Panel Sessions

Electronics Module Design and Reliability Prediction

**Presentation Abstract:** The presentation will focus on two case studies on the use of artificial intelligence/machine learning in automotive power electronics design from a thermal and mechanical standpoint, and alternative ways to develop a lifetime prediction model. In the first case study which uses a six-pack power module as an example, dimensionality reduction techniques are employed to identify the optimal parameters which can be used for design optimization studies.  The second one focuses on time-series forecasting techniques to predict the damage progression within a power module.

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**Professor Patrick McCluskey, University of Maryland**

**Bio:** Dr. Patrick McCluskey is a Professor of Mechanical Engineering at the University of Maryland, College Park and the Department's Director of Undergraduate Studies.  He has over 25 years of research experience in the areas of thermal management, reliability, and packaging of electronic systems for use in extreme temperature environments and power applications.  Dr. McCluskey has co-authored three books, 5 US Patents, and over 150 peer-reviewed technical articles with over 4500 citations. He is an associate editor of the IEEE Transactions on Components, Packaging, and Manufacturing Technology, a member of the board of governors of the IEEE Electronic Packaging Society, a fellow and member of the Executive Council of IMAPS, and a member of ASME and ASEE.

**Presentation Title:** Machine Learning in Reliability Assessment of Power Electronics for PV Inverters

**Presentation Abstract:** Conventional approaches to assess reliability of photovoltaic inverters have severe drawbacks. Frequent redesigns, often with new parts having no historical data, limit the usefulness of methods based on historical data. Conversely, physics-of-failure approaches often do not capture the most relevant failure mechanisms, including those related to operationally induced electrical overstress. In this presentation, we will discuss a revolutionary new reliability assessment approach that utilizes advancements in artificial intelligence (AI), machine learning, and data analytics, along with new techniques for characterizing and modeling failure mechanisms to improve power electronics reliability.  The reliability assessment method combines AI and machine learning algorithms for analyzing field failure data, with top down models that translate the impacts of grid-connected and grid-parallel mode dynamics and mode-transition dynamics on power systems, and reliability physics degradation models for key failure mechanisms that simulate the effects of both electrical and environmental degradation under field operational stresses. These models can be embedded in digital twins created specifically to replicate the design of current and new inverters. The output of these digital twins reflects the effects of aging and component degradation on system performance and will be transferable to multiple power electronic systems and platforms.

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**Dr. Mark Spector, Office of Naval Research**

**Bio:** Dr. Mark S. Spector is a Program Officer in the Sea Warfare and Weapons Department at the Office of Naval Research where he manages research in thermal science, metamaterials, energy conversion, and climate resilience.  In addition, he sits on the Steering Committee of the Department of Defense Energy and Power Community of Interest, the US Navy Climate Working Group, and the NATO Applied Vehicle Technology Power and Propulsion Systems Technical Committee.  Previously, he worked as a Research Physicist at the Naval Research Laboratory.  He received his doctorate in Physics from the Massachusetts Institute of Technology and bachelor's degrees in Physics and Applied Mathematics from the University of California at Berkeley.

**Presentation Title:** Machine Learning Methods for Thermal Management of Military Systems

**Presentation Abstract:** Modern military systems are trending towards significantly higher power loads with transient behavior that present unique challenges in thermal system design.  Electronics cooling based on convective heat transfer involves complex, nonlinear physics, where first principal calculations are often impractical.  Instead, empirical correlations are commonly used to predict heat transfer and fluid flow characteristics, but they are typically accurate only over a narrow range of geometric, heating, and flow conditions, which has hindered their widespread use for thermal system design.  Machine learning (ML) models offer the potential for a computationally inexpensive yet accurate way to model complex problems. ML studies of liquid-vapor phase change heat transfer to date have focused on developing supervised learning ML models as a replacement for empirical correlations.  While such models have improved prediction accuracies over empirical correlations, they cannot be generalized, are not scalable, and, thus, cannot be used to design more complex systems.  New physics-informed ML techniques that couple data sets with governing equations are needed to understand the thermofluidic behavior resulting in flow regime transitions and instabilities.

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**Professor Yoonjin Won, University of California, Irvine**

**Bio:** Yoonjin Won is currently an Associate Professor of Mechanical and Aerospace Engineering at the University of California, Irvine, with courtesy appointments in Electrical Engineering and Computer Science, and Materials Science Engineering. Dr. Won's research focuses on multiphase thermal science, integrating AI for science and experiment, scientific machine learning, and materials design. She leads the DoD funded multi-university research initiative, ML4Heat. She is a recipient of the National Science Foundation CAREER Award, the ASME Electronic & Photonic Packaging Division Early Career Award, the ASME Electronic & Photonic Packaging Division Women Engineer Award, the ASME ICNMM Outstanding Leadership Award, the Emerging Innovation/Early Career Innovator from UCI Beall Innovation Center, Faculty Excellence in Research Awards (Mid-Career) from UCI, and numerous best paper and poster awards. Yoonjin Won received her B.S. degree in Mechanical and Aerospace Engineering from Seoul National University, and her M.S. and Ph.D. degrees in Mechanical Engineering from Stanford University. For more information on Dr. Won's qualifications and research group, please visit won.eng.uci

**Presentation Title:** Applications of Machine Learning for Heat Transfer in Electronics Cooling

**Presentation Abstract:** Multiphase phenomena are observed in our everyday life in nature and many industrial applications, ranging from dew condensation on insects, water harvesting, electronics cooling, climatology prediction, hydrogen generations, and manufacturing. While the fundamentals of multiphase processes have been studied for over a century, key scientific questions remain regarding the fundamental mechanisms governing complex phenomena. The intricate interplay between the evolution of phase boundaries and mass transport results in nonlinear behavior, where subtle changes in one parameter can have profound and unexpected effects on others. The multimodal, multidimensional, and transient nature of these processes presents challenges for investigation and comprehension. Additionally, interpreting experimental data and predicting multiphase phenomena remain significant challenges. To address these challenges, our research group seeks to integrate cutting-edge computer vision and machine learning strategies. This talk will briefly discuss potential game-changing innovations for electronics cooling in heat transfer domain. I will highlight examples demonstrating how AI technologies enable learning, understanding, and prediction of the dynamic nature of multiphase phenomena. AI-driven algorithms can analyze vast amounts of data from sensors embedded in electronic devices, predicting thermal behaviors and dynamically adjusting cooling mechanisms. Machine learning models can be trained to identify patterns in heat generation and dissipation, allowing for predictive cooling strategies, thus extending the lifespan of components and reducing wear on cooling systems.

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**Professor Sanghamitra Neogi, Univ. of Colorado, Boulder**

**Bio:** Sanghamitra Neogi is an Associate Professor at the Ann and H.J. Smead Department of Aerospace Engineering Sciences at the University of Colorado Boulder. Additionally, she is a Program Faculty at the Materials Science and Engineering Program at the University of Colorado Boulder. Prior to joining CU, she received her B.Sc. and M.Sc. in Physics from Jadavpur University, Kolkata, and Indian Institute of Technology, Kanpur, India, respectively. She received her Ph.D. in theoretical condensed matter physics from the Pennsylvania State University and was a postdoctoral research associate at the Max Planck Institute for Polymer Research, Mainz, Germany. Her research received mention in the Journal of Physics D: Applied Physics article "The 2022 applied physics by pioneering women: a roadmap," and IEEE Spectrum article "Physicists Teach AI to Simulate Atomic Clusters: Physics-informed machine learning might help verify microchips." She is leading the development of atomistic thermal model of microelectronic systems within the DARPA Thermonat program.

**Presentation Title:** Atom-to-Circuit Thermal Modeling of Microelectronic Structures Using Physics-Aware Machine Learning

**Presentation Abstract:** The emerging deeply scaled transistors (<10 nm) include multiple materials and interfaces with dimensions on the order of nanometers. Thermal transport processes in such nanometer-scale materials can be drastically different from their bulk counterparts. The state-of-the-art thermal modeling of microelectronic structures that include increasingly large number of nanometer-scale transistors, are carried out using parametric continuum equation-based approaches. The models predict the temperature distributions generated due to self-heating but cannot explain thermal bottlenecks or runaways or reveal any mitigation strategies. Additionally, the time and resource costs for model calibrations are becoming increasingly large, especially for ultra-dense microelectronic structures. On the other hand, first-principles atomistic simulations can accurately predict thermal properties of the nanometer-scale materials. However, these simulations are not used for thermal modeling of microelectronic structures since the computation usually requires days to weeks for even simple structures. To overcome this challenge, we develop a new atom-to-circuit multi-scale modeling framework by inserting physics insights in machine learning (ML) models at different length scales. We combine phonon-physics insights, first-principles density functional theory calculations and large-scale molecular dynamics using machine learned potentials for expedited prediction of thermal properties of nanometer-scale transistors. We integrate the insight from the atomistic-ML simulations with finite element analysis and generative ML models for predicting heat map of millimeter-scale circuit elements based on circuit activities. The multi-scale framework not only predicts thermal properties of isolated nanometer-scale transistors but models heating and cooling of circuits including large number (>300,000) of nanometer-scale transistors. Thus, our framework illustrates an effective pathway to bridge physics insights from smaller length scales to continuum length scales and model thermal behavior of dense microelectronic structures.

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**Dr. Connor McCllelan, CEO, DeepSim Inc.**

**Bio:** Connor McClellan is the CEO of DeepSim, a Y Combinator-backed startup developing AI-accelerated physics simulation technology. At DeepSim, he leads the development of the Mariana simulator, which uses AI and GPU acceleration to deliver 1000X faster simulations than conventional FEM tools. Connor received a Ph.D. and M.S. in EE at Stanford University in 2021 and a B.S. in ECE at the University of Texas Austin in 2015.

**Presentation Title:** AI and GPU Acceleration to Overcome Semiconductor Simulation Scaling Challenges

**Presentation Abstract:** Transistor scaling and 3D integration have led to high power densities and operating temperatures, which degrade circuit reliability and performance. Layout complexities and nanoscale features have also made temperature difficult to measure, manage, and predict. Thus, new modeling approaches are needed to simulate temperature accurately and efficiently from nanoscale transistors to systems. To address this, we have developed the first AI-accelerated, multiscale, atoms-to-circuits thermal simulation pipeline, which we briefly outline here. Our pipeline begins with ab initio, atomistic materials modeling to extract nanoscale thermal properties, which we feed into a transistor thermal model. We then use this model in our transistors-to-circuits thermal simulation engine to predict the full-detail, nanoscale resolution temperature map of an active RISC-V core in < 10 minutes. Ultimately, our atoms-to-circuits thermal simulation pipeline enables engineers across the physical design process to accurately and rapidly evaluate the impact of heat on their designs.

# Committee Meetings

| TUESDAY, OCTOBER 8 | | |
|---|---|---|
| TIME | Meeting | Room |
| 7:00PM–8:00PM | K-16 Committee Meeting | Offsite - TBA |
| **WEDNESDAY, OCTOBER 9** | | |
| 5:45PM–6:45PM | InterPACK Closed Meeting | California Ballroom - Salon D |
| 5:45PM–6:45PM | InterPACK Open Meeting | California Ballroom - Salon D |
| 6:45 PM–7:15 PM | K-16 Committee Meeting (Open) | California Ballroom, Salon D |
| 7:00PM–8:00PM | InterPACK EPPD Meeting | California Ballroom - Salon D |
| 7:45 PM–9:15 PM | K-16 Committee Meeting (Closed) | California Ballroom - Salon D |

**All technical presentations will be available on the Conference Application (App) and available for download. Check your emails for access or scan the QR code at Registration.**

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| 02-04 Data Center Cooling I | Warzoha | Ron | United States Naval Academy |
| 02-05 Data Center Cooling II | Modi | Himanshu | University of Texas at Arlington \| UTA |
| 02-05 Data Center Cooling II | Kasukurthy | Rajesh | ECS |
| 03-01 Solder Joints and Reliability I | Kothari | Nakul | Qualcomm |
| 03-02 Solder Joints and Reliability II | Shahi | Pardeep | NVIDIA |
| 03-03 Thermal Management and Reliability I | Harsha | Mahendra | Qualcomm |
| 03-04 Thermal Management and Reliability II | Shahi | Pardeep | NVIDIA |
| 03-05 Stress Modeling and Reliability | Harsha | Mahendra | Qualcomm |
| 03-06 Power Electronic Modules and Reliability | Kothari | Nakul | Qualcomm |
| 03-07 Sintered Attach and Additive Manufacturing | Kothari | Nakul | Qualcomm |
| 03-08 Measurement of Properties and Characteristics | Shahi | Pardeep | NVIDIA |
| 03-09 Device and Materials Reliability | Shahi | Pardeep | NVIDIA |
| 04-01 Power/RF Electronics and Photonics I | Chatterjee | Bikramjit | Lawrence livermore national laboratory |
| 04-02 Power/RF Electronics and Photonics II | Donmezer | Nazli | Bogazici University |
| 04-03 Power/RF Electronics and Photonics III | Fish | Michael | Army Research Laboratory |
| 04-04 Power/RF Electronics and Photonics IV | Yuruker | Sevket | Tesla |
| 04-05 Power/RF Electronics and Photonics V | Zhang | Winston | University of Illinois at Urbana-Champaign |
| 04-06 Power/RF Electronics and Photonics VI | Cho | Jungwan | Sungkyunkwan University |
| 05-01 Nanoscale Thermal Transport Processes in Electronic Systems | Warzoha | Ron | United States Naval Academy |

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| 05-02 Nanoscale and Microscale Thermal Conduction Phenomena in Electronic Materials | Donovan | Brain | United States Naval Academy |
| 05-03 Single-phase and Two-phase Flow | Padilla | Jorge | Google |
| 05-04 Phase Change Materials and Transient Thermal Management | Wilson | Adam | Army Research Laboratory |
| 05-05 Thermal Transport Phenomena in Emerging Technologies | Miljkovic | Nenad | University of Illinois at Urbana-Champaign |
| 05-05 Thermal Transport Phenomena in Emerging Technologies | Kim | Dohwan | Qualcomm |
| 05-06 Nanoscale Thermal Transport Processes in Electronic Systems II | Wilson | Adam | US Army Research Laboratory |
| 05-07 Nanoscale and Microscale Thermal Conduction Phenomena in Electronic Materials II | Jang | Hyejin | Seoul National University |
| 05-08 Single-Phase and Two-Phase Flow II | Warzoha | Ronald | United States Naval Academy |
| 05-09 Phase Change Materials and Transient Thermal Management II | Miljkovic | Nenad | University of Illinois At Urbana-Champaign |
| 05-10 Thermal Transport Phenomena in Emerging Technologies II | Padilla | Jorge | Google LLC |
| 06-01 Wearable Electronics | Kim | Kyungjin Kim | University of Connecticut |
| 06-02 Reliability & Repairability of Additive Electronics | Lall | Pradeep | Auburn University |
| 06-03 Print Process Optimization I | Hines | Daniel | Raytheon Technologies |
| 06-04 Print Process Optimization II | Paquette | Beth | NASA |
| 06-05 Advanced Processing & Modeling for Printed & Flexible Electronics | LEEVER | Benjamin | Air Force Research Laboratory |
| 06-06 FHE Processing & Component Attach | LEEVER | Benjamin | Air Force Research Laboratory |
| 06-06 In-Mold Electronics | Hines | Daniel | Raytheon Technologies |
| 07-01 AI/ML-assisted design for manufacturability and reliability | Weiner | Joyce | Intel Corporation |
| 07-02 Design for manufacturability and reliability in transportation applications | Welschinger | Fabian | Robert Bosch GmbH |
| 07-03 Reliability of polymers and interfaces | Weiner | Joyce | Intel Corporation |
| 07-04 Reliability of interfaces | Gromala | Przemyslaw | Robert Bosch GmbH |
| 07-05 Reliability of solders | Weiner | Joyce | Intel Corporation |
| 08-01 Interactive Presentations | Pavlidis | Georges | University of Connecticut |
| 08-01 Interactive Presentations | Adera | Solomon | University of Michigan |
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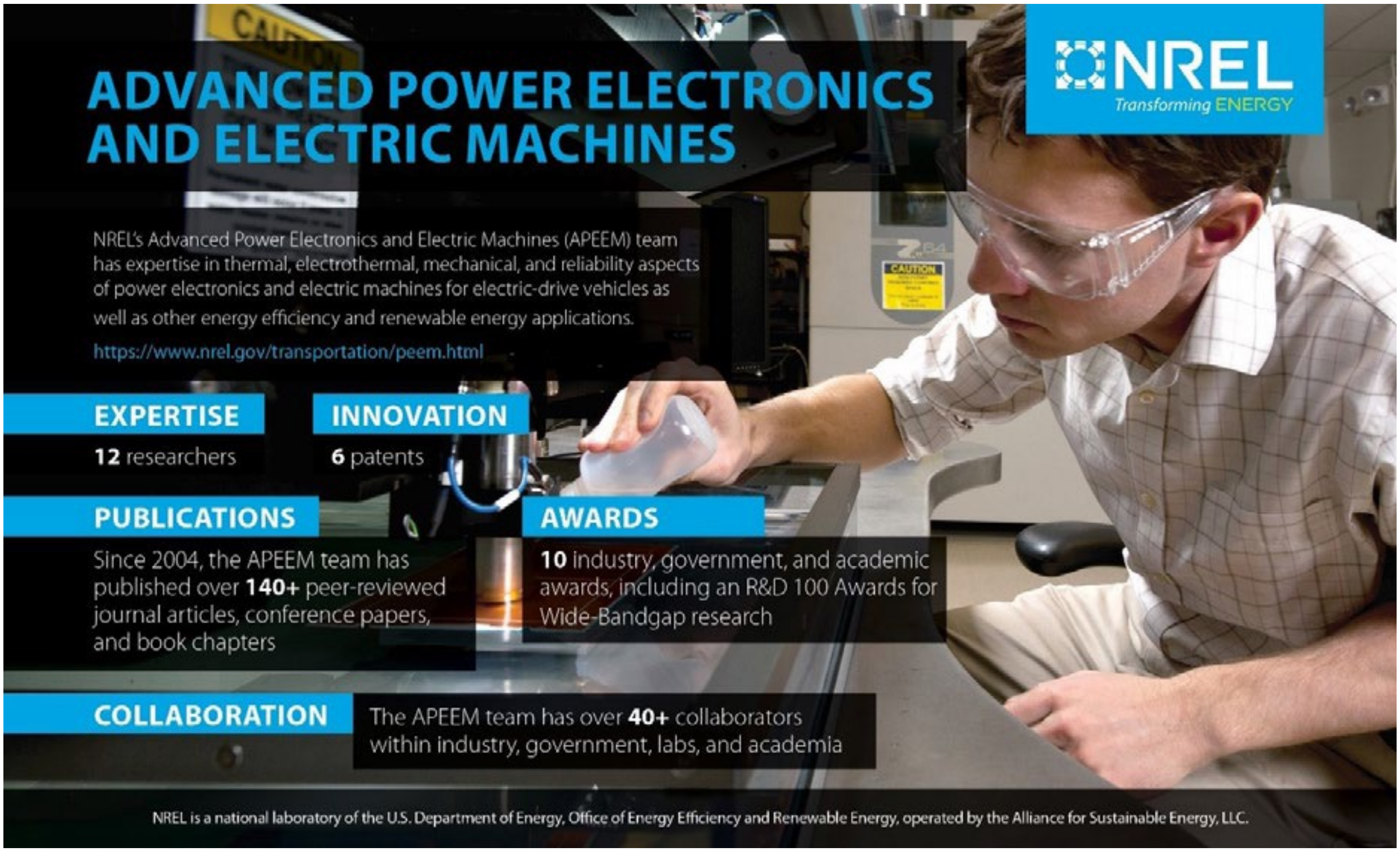


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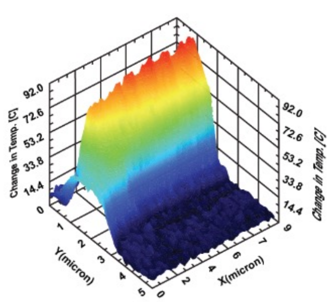


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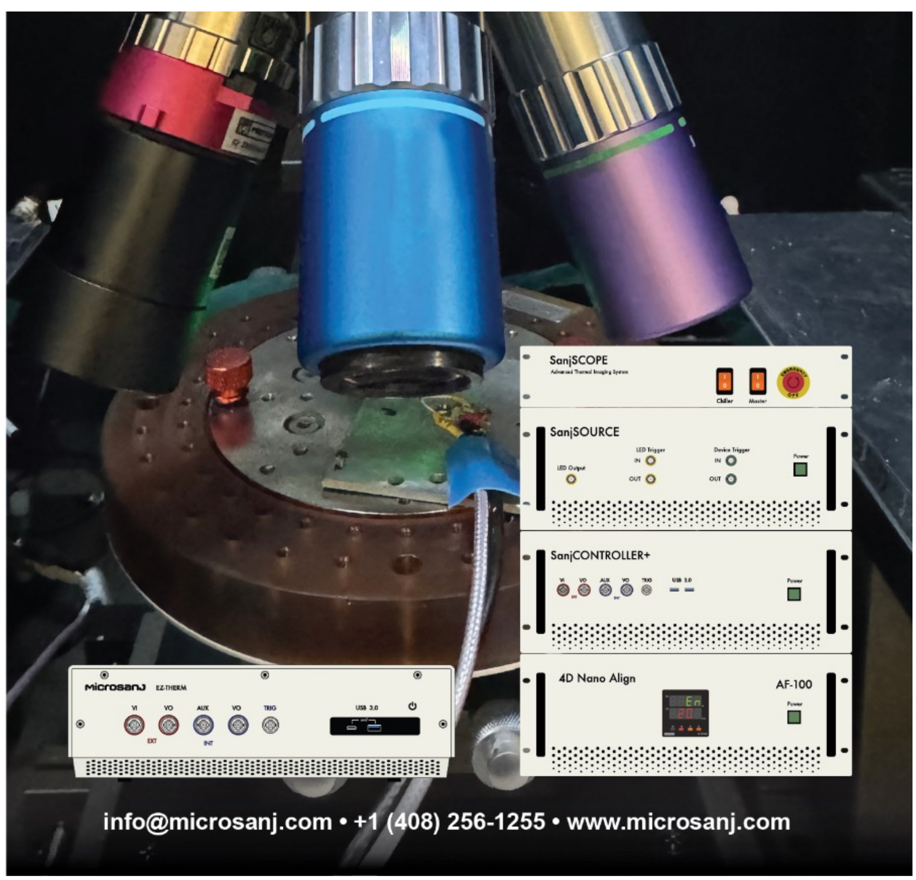

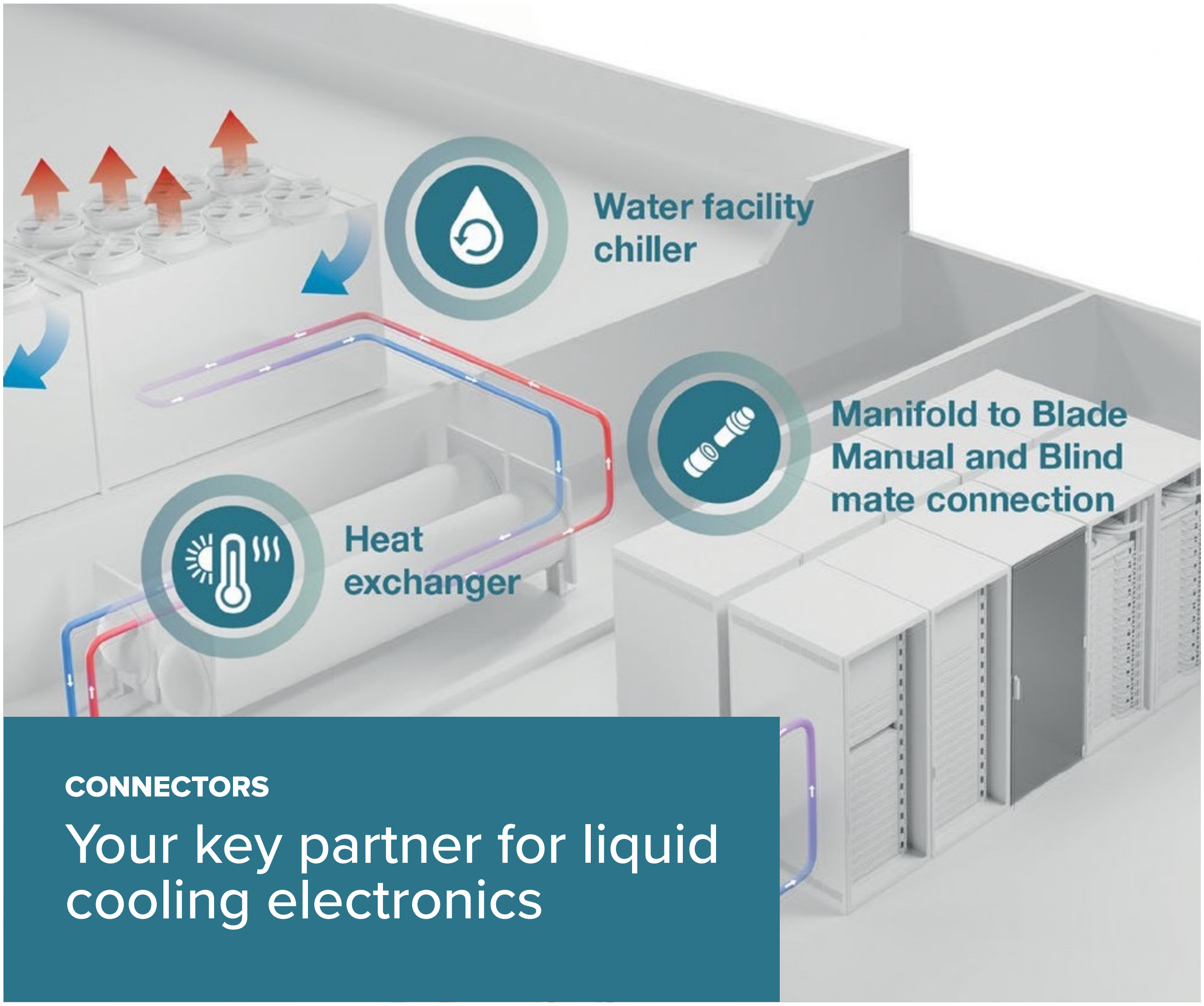


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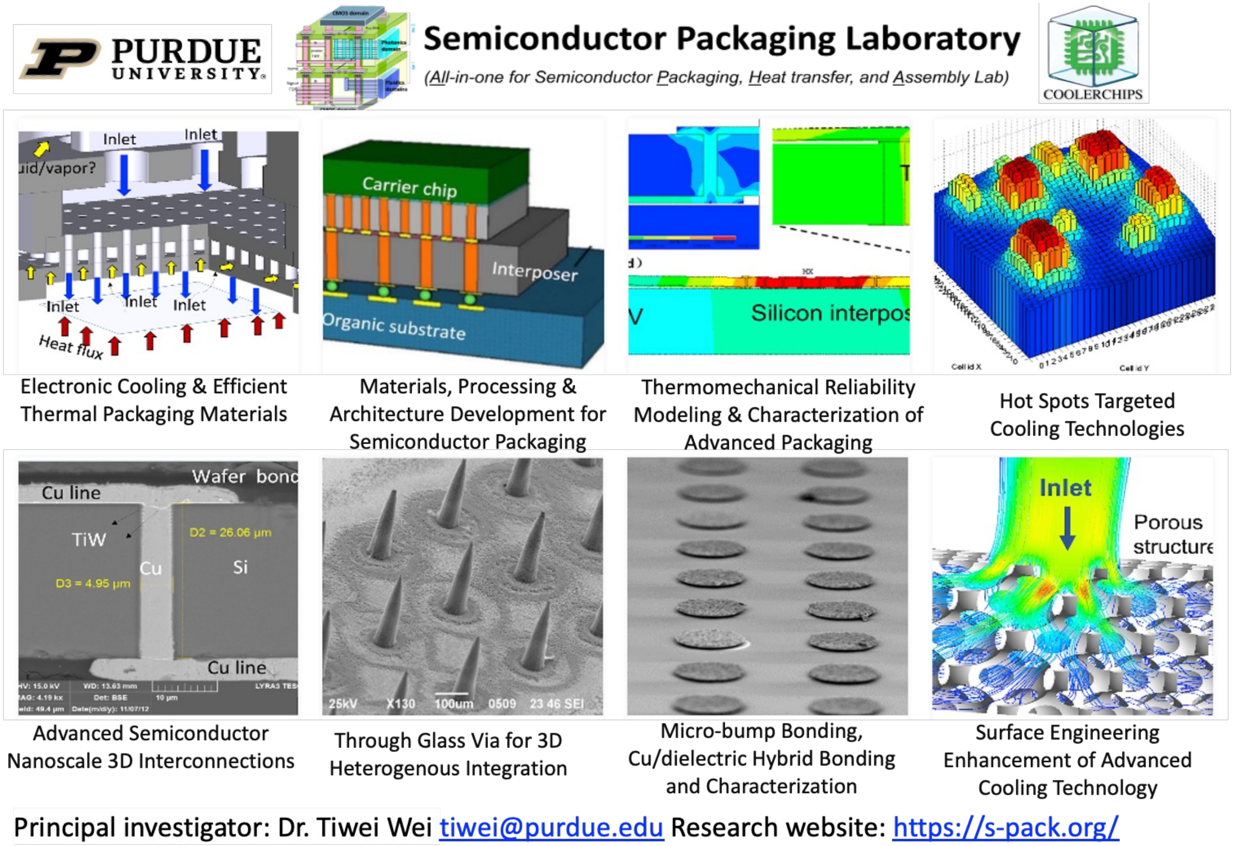


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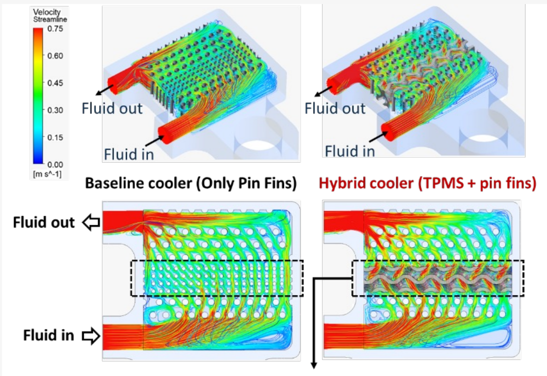
https://mettl.gatech.edu/




Hybrid pin fin and TPMS architecture cold plate for electronics thermal management

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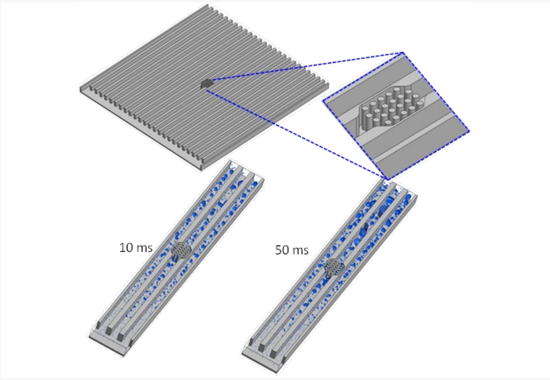
https://sites.gatech.edu/minds/




Spatial vapor distribution at different time instants from CFD simulations. Flowrate: 0.06 L/min, and hot spot heat flux: 120 W/cm2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Two-phase immersion cooling of electronics
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Thermal modeling tools for datacenter digital twin
PINN for hotspot prediction of GaN devices
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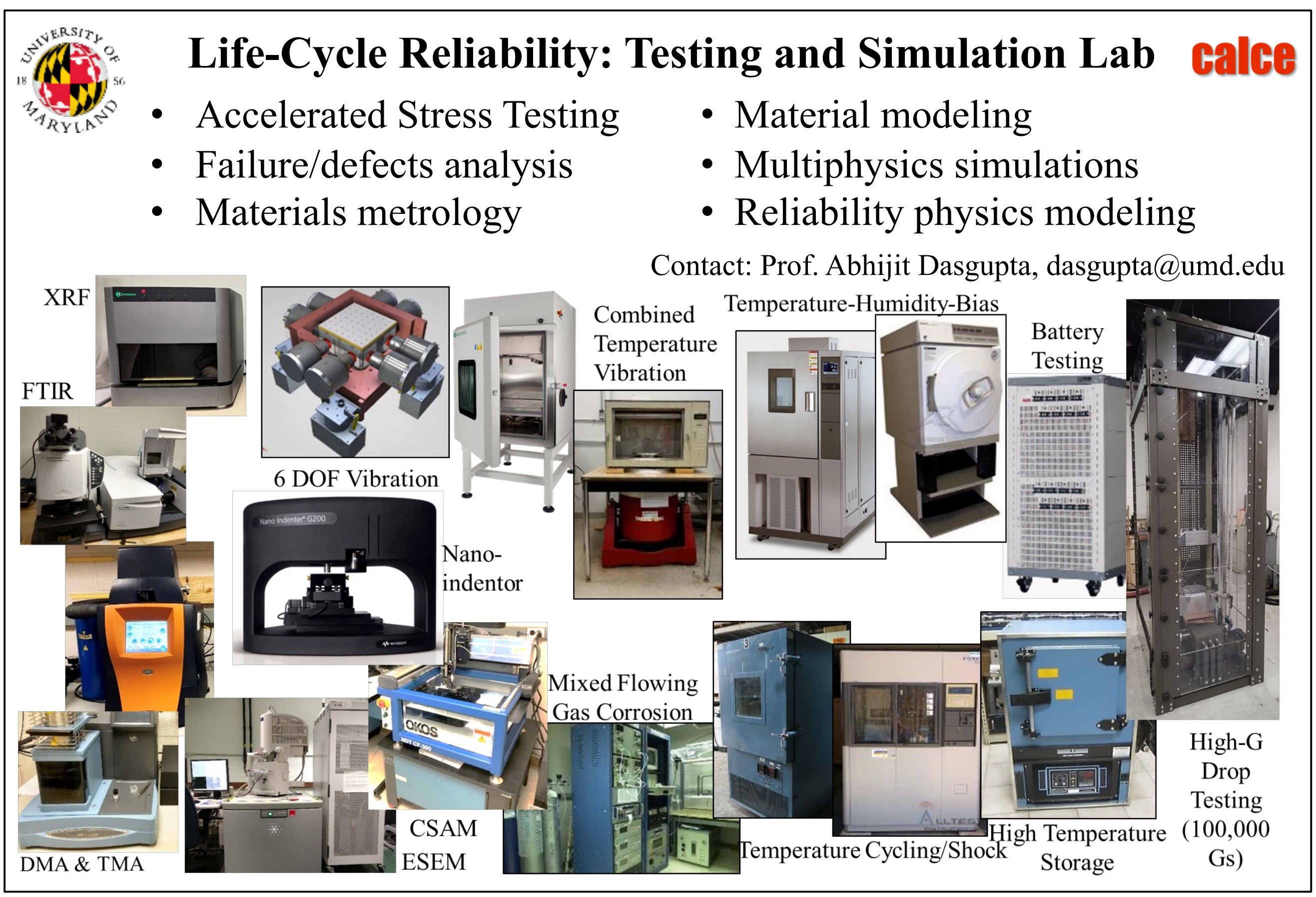
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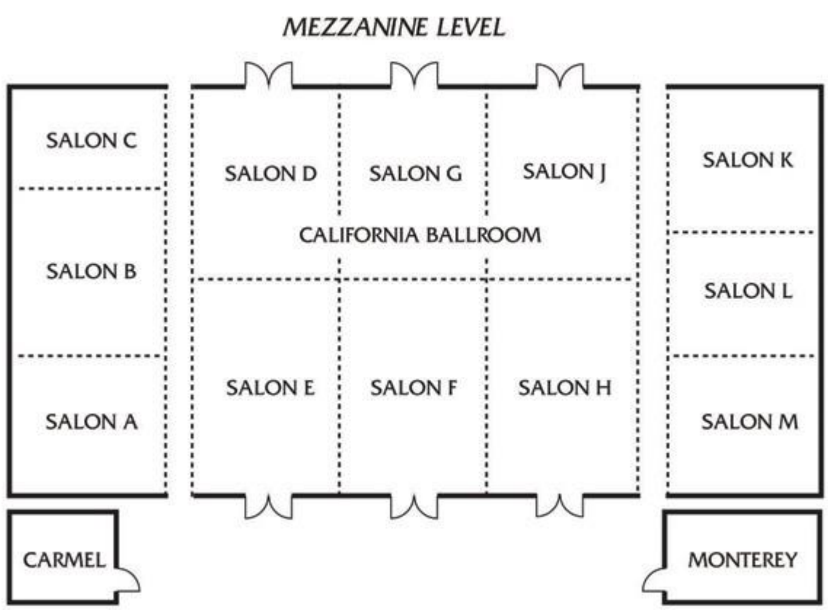


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